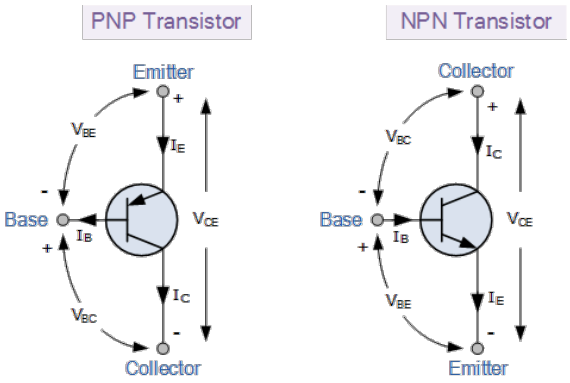
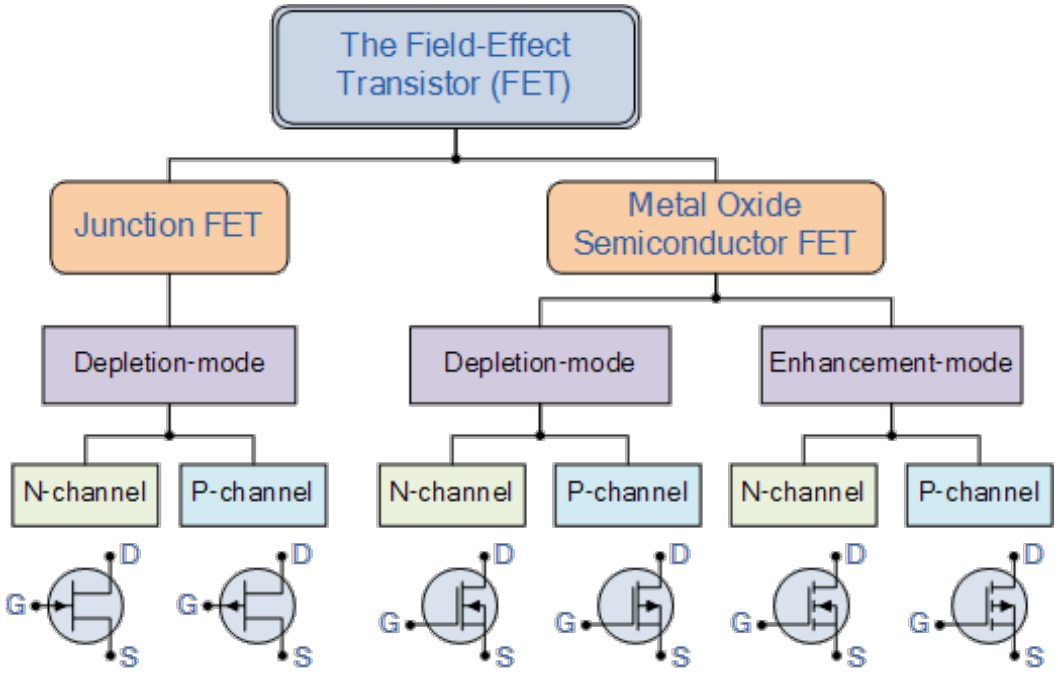


- Transistors are "**Current Operated Devices**" where a much smaller Base current causes a larger Emitter to Collector current, which themselves are nearly equal, to flow.
- Requires a Biasing voltage for AC amplifier operation.
- The Base-Emitter junction is always forward biased whereas the Collector-Base junction is always reverse biased.

- The standard equation for currents flowing in a transistor is given as: $I_E = I_B + I_C$
- The Collector or output characteristics curves can be used to find either Ib, Ic or β to which a load line can be constructed to determine a suitable operating point, Q with variations in base current determining the operating range.
- **Field Effect Transistors**, or FET's are "**Voltage Operated Devices**" and can be divided into two main types: Junction-gate devices called JFETs and Insulated-gate devices called IGFETs or more commonly known as MOSFETs, which can also be sub-divided into Enhancement types and Depletion types. All forms are available in both N-channel and P-channel versions.
- The input impedance of the MOSFET is even higher than that of the JFET due to the insulating oxide layer and therefore static electricity can easily damage MOSFET devices.
- When no voltage is applied to the gate of an enhancement FET the transistor is in the "OFF" state similar to an "open switch".
- The depletion FET is inherently conductive and in the "ON" state when no voltage is applied to the gate similar to a "closed switch".
- To turn the N JFET transistor OFF, a negative voltage must be applied to the gate.
- To turn the P JFET transistor OFF, a positive voltage must be applied to the gate.
- N-channel depletion MOSFETs are in the "OFF" state when a negative voltage is applied to the gate to create the depletion region.
- P-channel depletion MOSFETs, are in the "OFF" state when a positive voltage is applied to the gate to create the depletion region.
- Nel enhancement MOSFETs are in the "ON" state when a "+ve" (positive) voltage is applied to the gate.
- P enhancement MOSFETs are in the "ON" state when "-ve" (negative) voltage is applied to the gate.



Biasing of the Gate :

Type	Junction FET		Metal Oxide Semiconductor FET			
	Depletion Mode		Depletion Mode		Enhancement Mode	
Bias	ON	OFF	ON	OFF	ON	OFF
N-channel	0v	-ve	0v	-ve	+ve	0v
P-channel	0v	+ve	0v	+ve	-ve	0v

The Field Effect Transistor

The **Field Effect Transistor**, or simply **FET** however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the **Field Effect Transistor** a "VOLTAGE" operated device.

The field effect transistor is a three terminal device that is constructed with no PN-junctions within the main current carrying path between the Drain and the Source terminals, which correspond in function to the Collector and the Emitter respectively of the bipolar transistor. The current path between these two terminals is called the "channel" which may be made of either a P-type or an N-type semiconductor material.

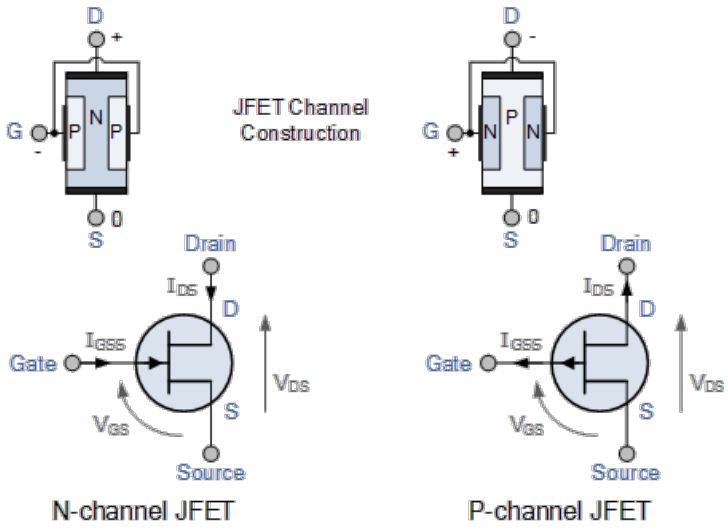
The control of current flowing in this channel is achieved by varying the voltage applied to the Gate. As their name implies, Bipolar Transistors are "Bipolar" devices because

they operate with both types of charge carriers, Holes and Electrons. The Field Effect Transistor on the other hand is a "Unipolar" device that depends only on the conduction of electrons (N-channel) or holes (P-channel).

There are two main types of field effect transistor, the **Junction Field Effect Transistor** or **JFET** and the **Insulated-gate Field Effect Transistor** or **IGFET)**, which is more commonly known as the standard **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The Junction Field Effect Transistor

We saw previously that a bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The **Junction Field Effect Transistor** has no PN-junctions but instead has a narrow piece of high resistivity semiconductor material forming a "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source respectively.



There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts.

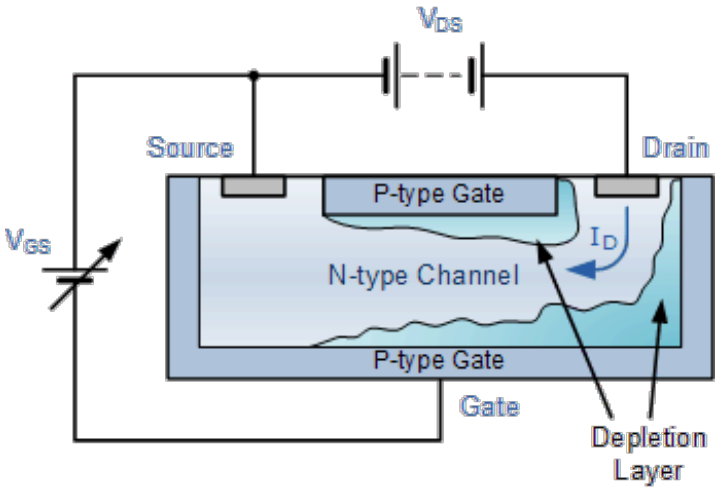
The semiconductor "channel" of the **Junction Field Effect Transistor** is a resistive path through which a voltage V_{DS} causes a current I_D to flow and as such the junction field effect transistor can conduct current equally well in either direction. As the channel is

resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal.

The result is that the PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a “depletion layer” to be formed within the channel and whose width increases with the bias.

The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive. The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Biasing of an N-channel JFET



The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the *depletion region* around the Gate area when no external voltages are applied. JFETs are therefore known as depletion mode devices.

This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself.

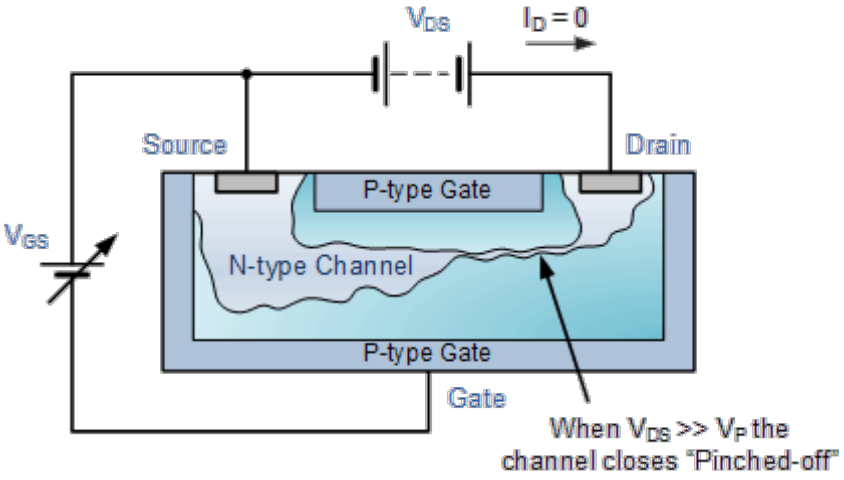
Then we can see that the most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET’s channel conducts with zero bias voltage applied (ie, the depletion region has near zero width).

With no external Gate voltage ($V_G = 0$), and a small voltage (V_{DS}) applied between the Drain and the Source, maximum saturation current (I_{DSS}) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

If a small negative voltage (-V_{GS}) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of “squeezing” effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage (-V_{GS}) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be “pinched-off” (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the “pinch-off voltage”, (V_P).

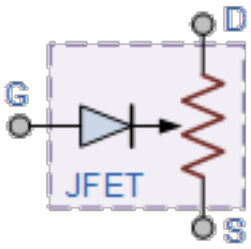
JFET Channel Pinched-off



In this pinch-off region the Gate voltage, V_{GS} controls the channel current and V_{DS} has little or no effect.

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when $V_{GS} = 0$ and maximum “ON” resistance R_{DS} when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.

It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

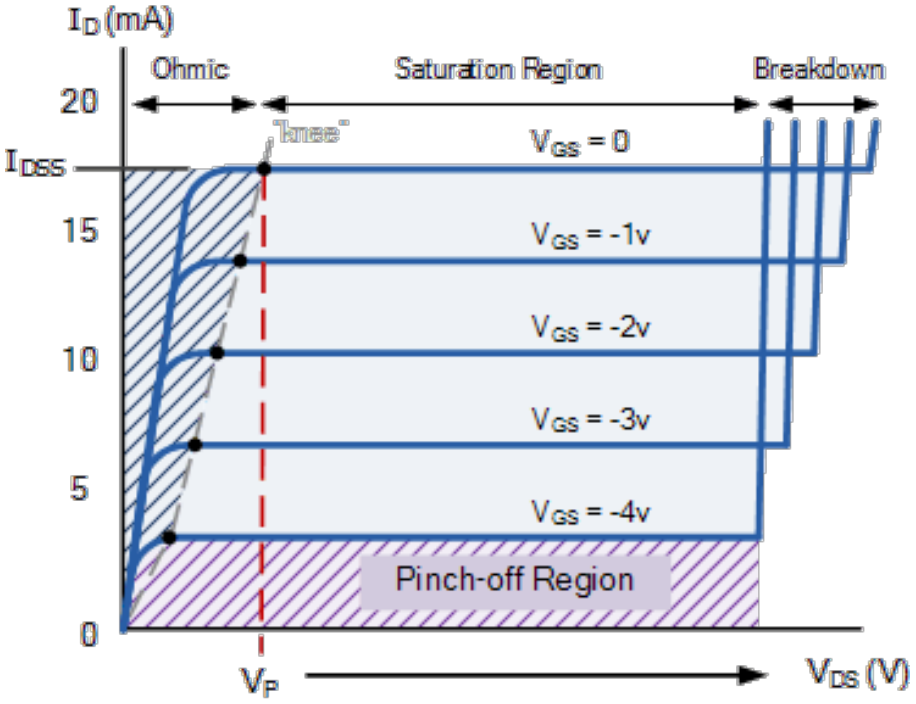


- No Gate voltage (V_{GS}) and V_{DS} is increased from zero.
- No V_{DS} and Gate control is decreased negatively from zero.
- V_{DS} and V_{GS} varying.

The P-channel **Junction Field Effect Transistor** operates the same as the N-channel above, with the following exceptions: 1). Channel current is positive due to holes, 2). The polarity of the biasing voltage needs to be reversed.

The output characteristics of an N-channel JFET with the gate short-circuited to the source is given as :

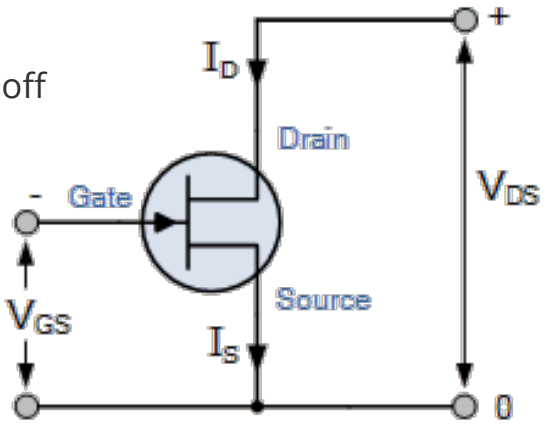
Output characteristic V-I curves of a typical junction FET



Because a **Junction Field Effect Transistor** is a voltage controlled device, no current flows into the gate, then the Source current I_S flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

- Ohmic Region – When $V_{GS} = 0$ the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
- Cut-off Region – This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.



- Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
- Breakdown Region – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

The Drain current is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and I_{DSS} (maximum current). By knowing the Drain current I_D and the Drain-Source voltage V_{DS} the resistance of the channel (I_D) is given as:

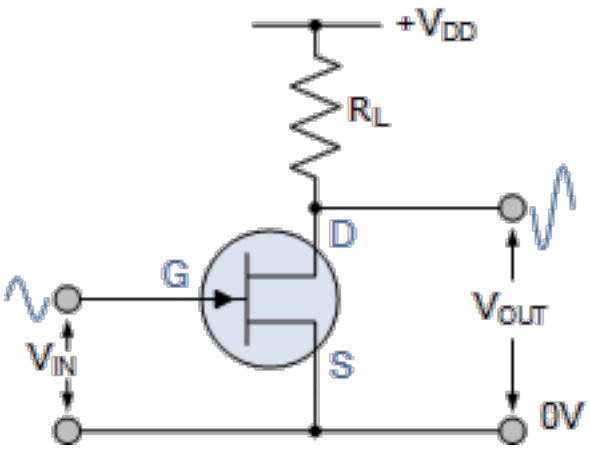
$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where g_m is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

Modes of FET's

The principals of operation for a P-channel JFET are the same as for the N-channel JFET, except that the polarity of the voltages need to be reversed.

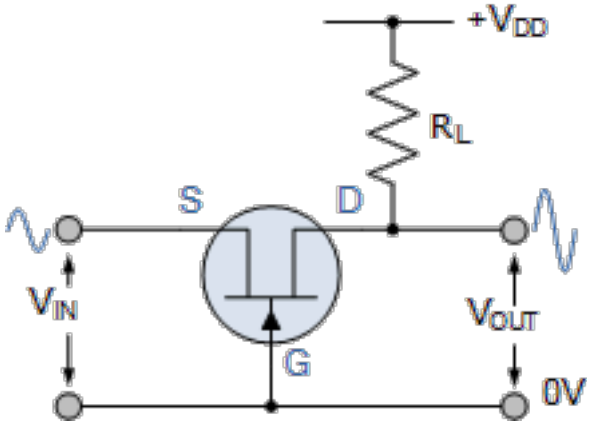
Common Source (CS) Configuration



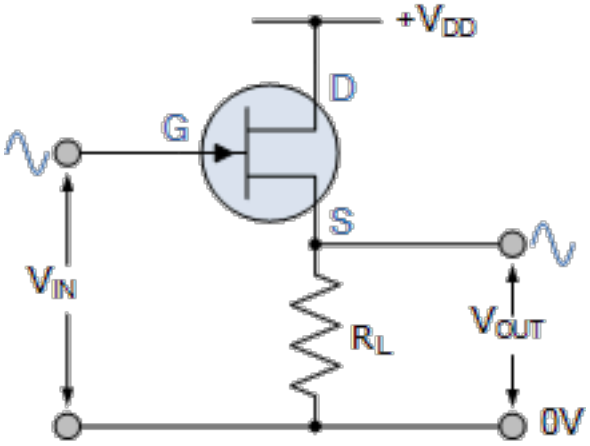
In the **Common Source** configuration (similar to common emitter), the input is applied to the Gate and its output is taken from the Drain as shown. This is the most common mode of operation of the FET due to its high input impedance and good voltage amplification and as such Common Source amplifiers are widely used. The common source mode of FET connection is generally used audio frequency amplifiers and in high input impedance pre-amps and stages. The output signal is 180° "out-of-phase" with the input.

Common Gate (CG) Configuration

In the **Common Gate** configuration (similar to common base), the input is applied to the Source and its output is taken from the Drain with the Gate connected directly to ground (0v) as shown. The high input impedance feature of the previous connection is lost in this configuration as the common gate has a low input impedance, but a high output impedance. This type of FET configuration can be used in high frequency circuits or in impedance matching circuits.



Common Drain (CD) Configuration



In the **Common Drain** configuration (similar to common collector), the input is applied to the Gate and its output is taken from the Source. The common drain or "source follower" configuration has a high input impedance and a low output impedance and near-unity voltage gain so is therefore used in buffer amplifiers. The voltage gain of the source follower configuration is less than unity, and the output signal is "in-phase" with the input signal. This type of configuration is referred to as "Common Drain" because there is no signal available at the drain connection, the voltage present, $+V_{DD}$ just provides a bias.

The JFET Amplifier

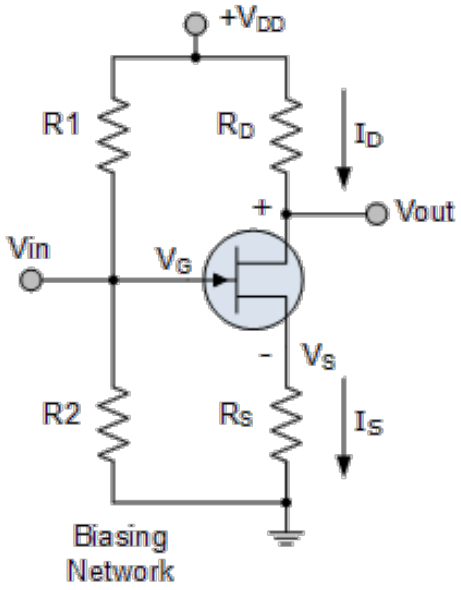
Just like the bipolar junction transistor, JFET's can be used to make single stage class A amplifier circuits with the JFET common source amplifier and characteristics being very similar to the BJT common emitter circuit. The main advantage JFET amplifiers have over BJT amplifiers is their high input impedance which is controlled by the Gate biasing resistive network formed by R1 and R2 as shown.

$$V_S = I_D R_S = \frac{V_{DD}}{4}$$

$$V_S = V_G - V_{GS}$$

$$V_G = \left(\frac{R2}{R1 + R2} \right) V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$



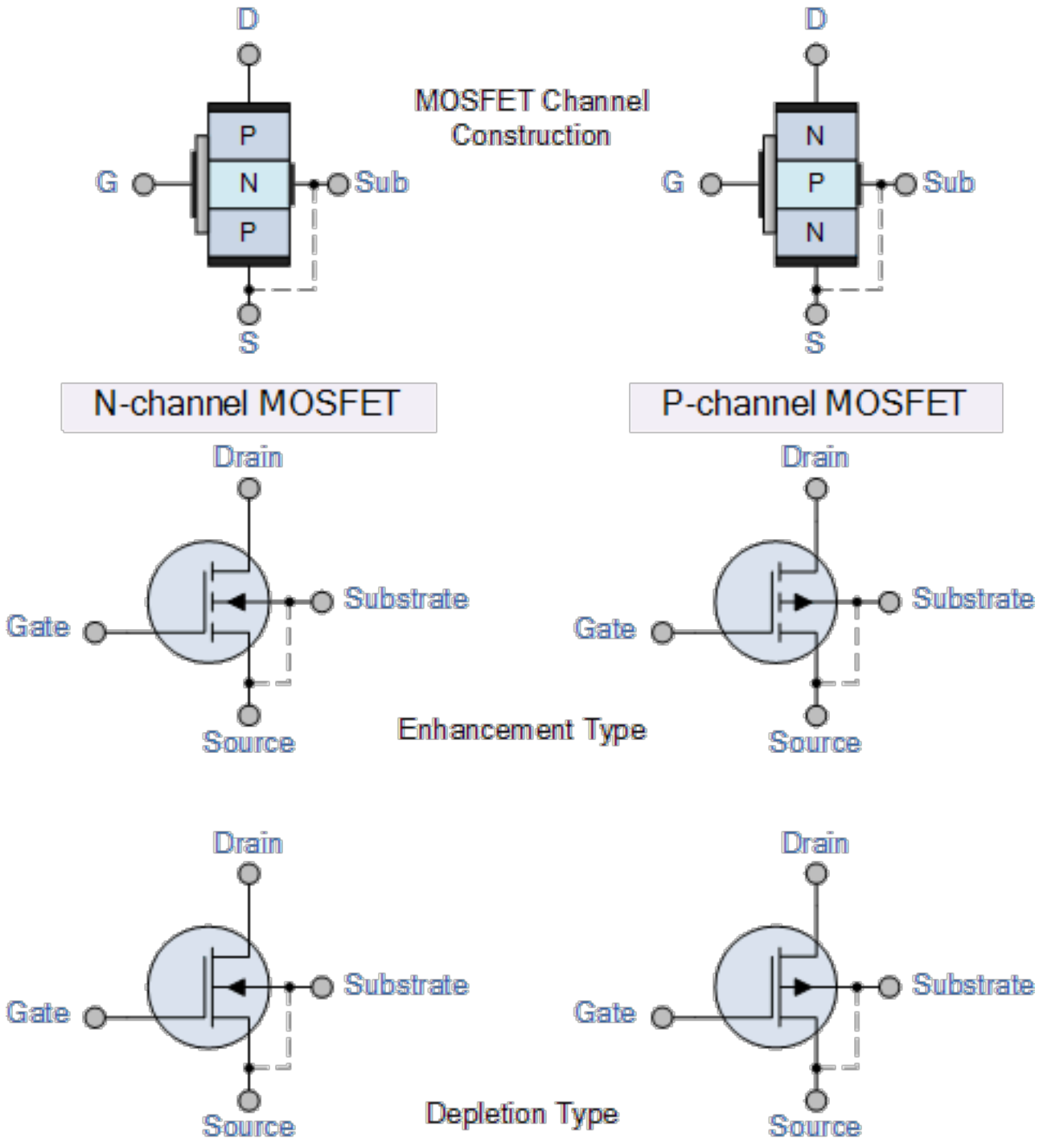
This common source (CS) amplifier circuit is biased in class “A” mode by the voltage divider network formed by resistors R1 and R2. The voltage across the Source resistor RS is generally set to be about VDD/4. The required Gate voltage can then be calculated using this RS value. Since the Gate current is zero, (IG = 0) we can set the required DC quiescent voltage by the proper selection of resistors R1 and R2.

The MOSFET

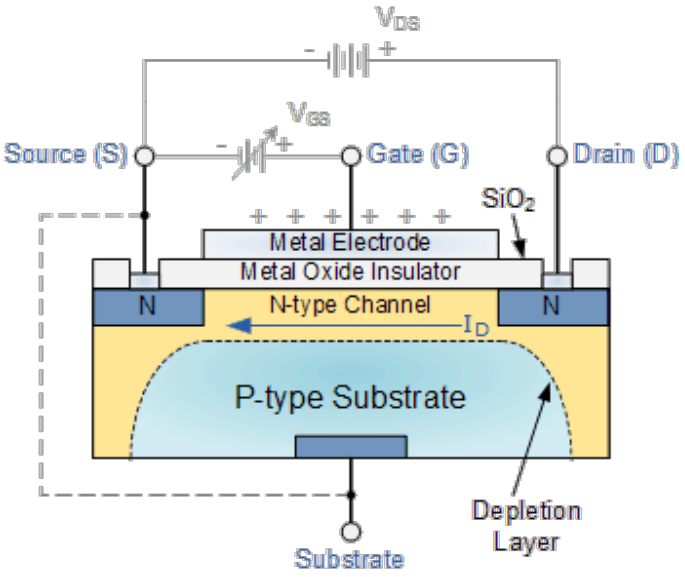
The **IGFET** or **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor N-channel or P-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass. This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor, so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve). The isolation of the controlling Gate makes the input resistance of the **MOSFET** extremely high way up in the MΩ region thereby making it almost infinite.

MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

- Depletion Type – The transistor requires the Gate-Source voltage (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.
- Enhancement Type – The transistor requires a Gate-Source voltage (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.



The four MOSFET symbols above show an additional terminal called the Substrate and is not normally used as either an input or an output connection but instead it is used for grounding the substrate. It connects to the main semiconductive channel through a diode junction to the body or metal tab of the MOSFET. Usually in discrete type MOSFETs, this substrate lead is connected internally to the source terminal.



The electrical field produced by the gate voltage alter the flow of charge carriers, electrons for N-channel or holes for P-channel, through the semiconductive drain-source channel.

MOSFETs have the ability to operate within three different regions:

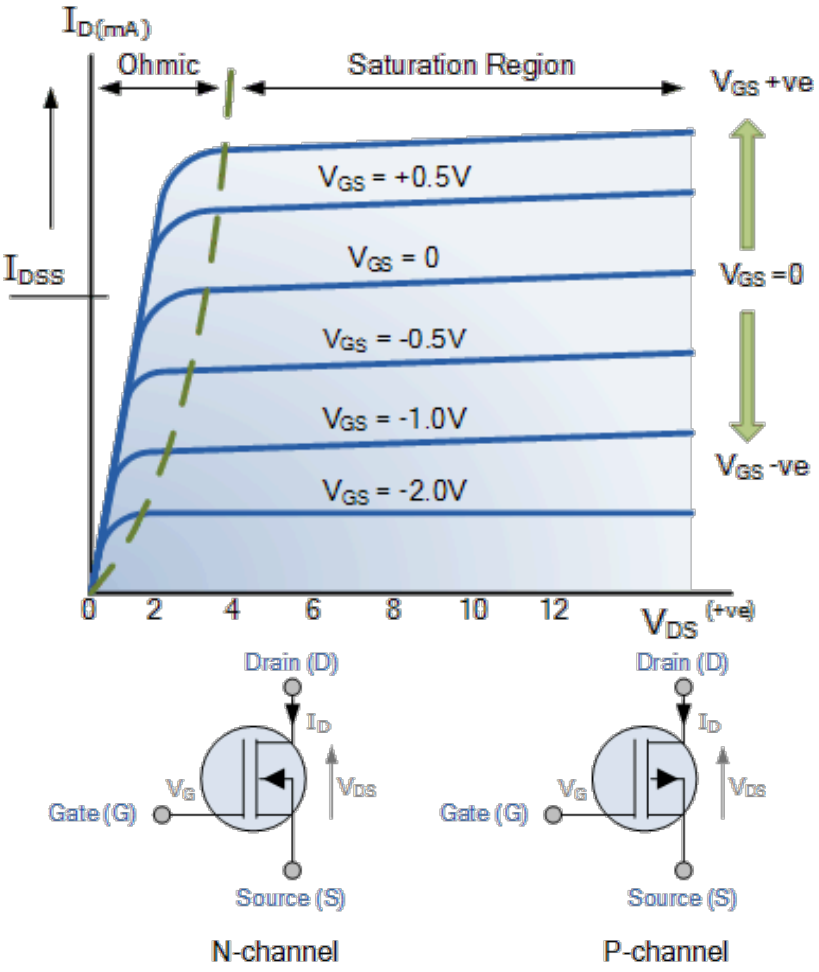
- Cut-off Region – with $V_{GS} < V_{threshold}$ the gate-source voltage is lower than the threshold voltage so the MOSFET transistor is switched "fully-OFF" and $I_{DS} = 0$, the transistor acts as an open circuit
- Linear (Ohmic) Region – with $V_{GS} > V_{threshold}$ and $V_{DS} > V_{GS}$ the transistor is in its constant resistance region and acts like a variable resistor whose value is determined by the gate voltage, V_{GS}
- Saturation Region – with $V_{GS} > V_{threshold}$ the transistor is in its constant current region and is switched "fully-ON". The current I_{DS} = maximum as the transistor acts as a closed circuit

The voltage point at which the MOSFET starts to pass current through the channel is determined by the threshold voltage V_{TH} of the device and is typical around 0.5V to 0.7V for an N-channel device and -0.5V to -0.8V for a P-channel device.

MOSFET type	V_{GS} = +ve	V_{GS} = 0	V_{GS} = -ve
N-Channel Depletion	ON	ON	OFF
N-Channel Enhancement	ON	OFF	OFF
P-Channel Depletion	OFF	ON	ON
P-Channel Enhancement	OFF	OFF	ON

Depletion-mode MOSFET

The **Depletion-mode MOSFET**, which is less common than the enhancement types is normally switched "ON" without the application of a gate bias voltage making it a "normally-closed" device. However, a gate to source voltage VGS will switch the device "OFF". For an N-channel MOSFET, a "positive" gate voltage widens the channel, increasing the flow of the drain current and decreasing the drain current as the gate voltage goes more negative.

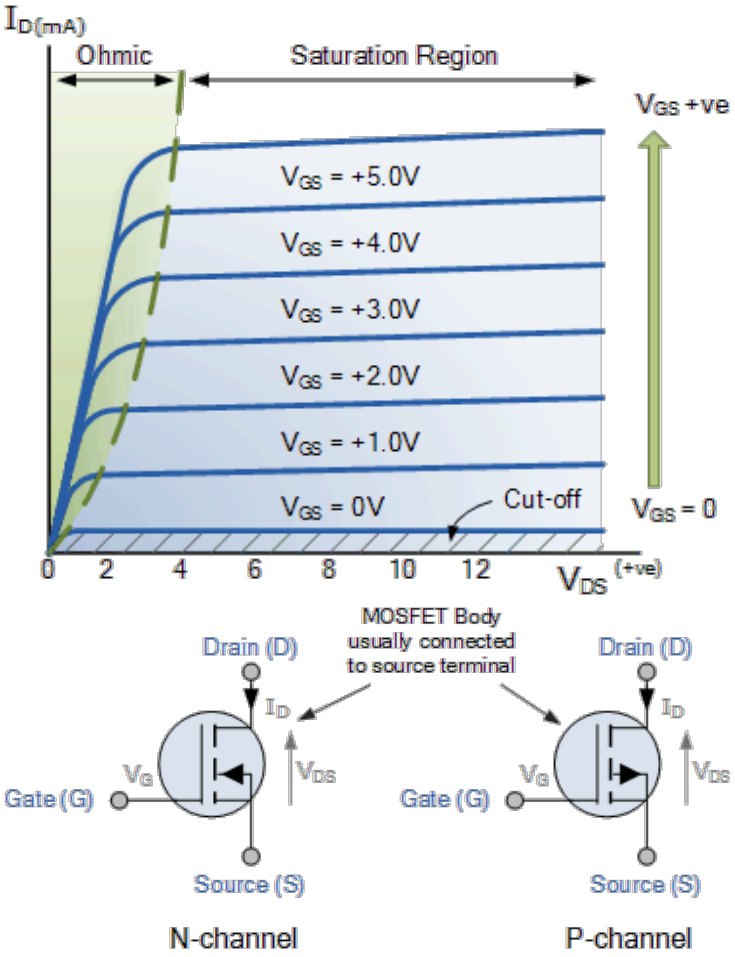


In other words, for an N-channel depletion mode MOSFET: +VGS means more electrons and more current. While a -VGS means less electrons and less current. The opposite is also true for the P-channel types. Then the depletion mode MOSFET is equivalent to a "normally-closed" switch.

The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts were the drain-source channel is inherently conductive with the electrons and holes already present within the N-type or P-type channel. This doping of the channel produces a conducting path of low resistance between the Drain and Source with zero Gate bias.

Enhancement-mode MOSFET

The more common **Enhancement-mode MOSFET** is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally "OFF" when the gate bias voltage is equal to zero.



A drain current will only flow when a gate voltage V_{GS} is applied to the gate terminal greater than the threshold voltage V_{TH} level in which conductance takes place making it a transconductance device. This positive +ve gate voltage pushes away the holes within the channel attracting electrons towards the oxide layer and thereby increasing the thickness of the channel allowing current to flow. This is why this kind of transistor is called an enhancement mode device as the gate voltage enhances the channel.

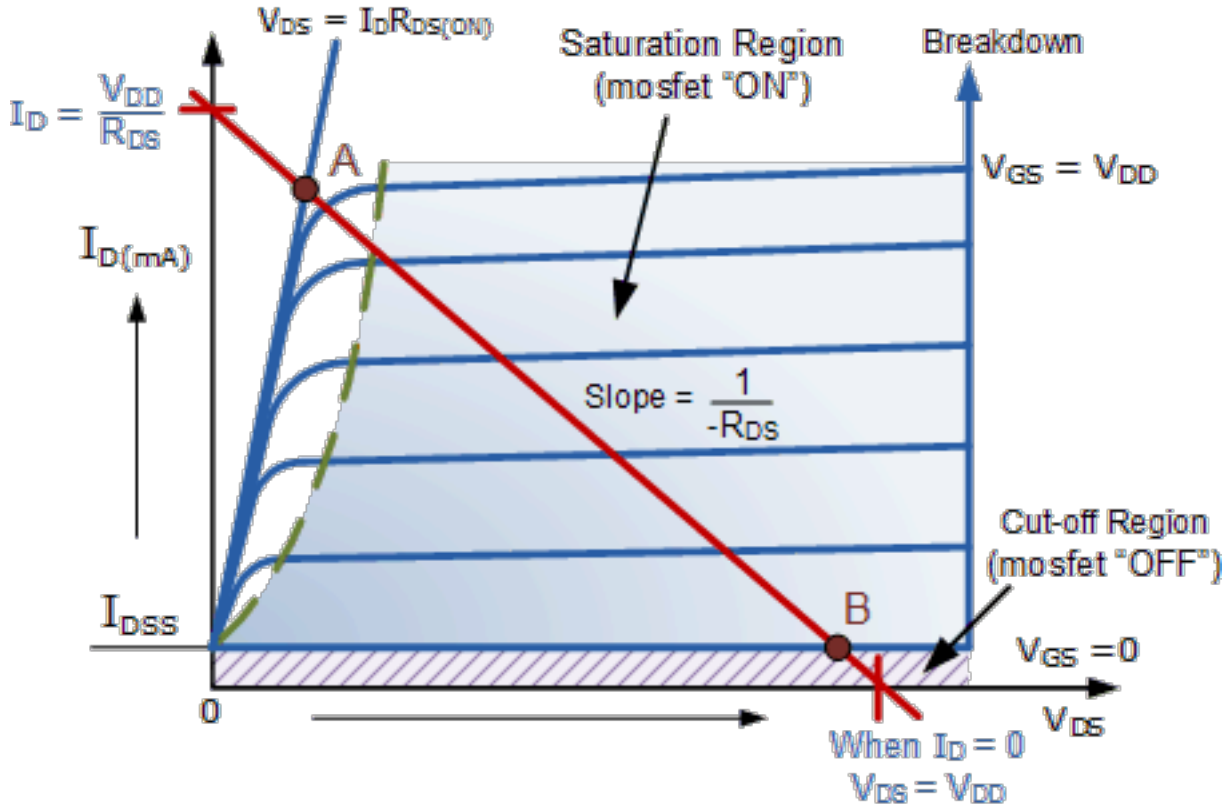
Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, I_D through the channel. In other words, for an N-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor "ON", while a zero or $-V_{GS}$ turns the transistor "OFF". Then, the enhancement-mode MOSFET is equivalent to a "normally-open" switch.

Enhancement-mode MOSFETs make excellent electronics switches due to their low "ON" resistance and extremely high "OFF" resistance as well as their infinitely high gate resistance. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type *Logic Gates* and power switching circuits in the form of as PMOS and NMOS gates.

The MOSFET as a Switch

In this tutorial we will look at using the *Enhancement-mode MOSFET as a Switch* as these transistors require a positive gate voltage to turn "ON" and a zero voltage to turn "OFF".

The operation of the e-MOSFET, can best be described using its I-V characteristics curves shown below. When the input voltage V_{IN} to the gate of the transistor is zero, the MOSFET conducts virtually no current and the output voltage V_{OUT} is equal to the supply voltage V_{DD}. So the MOSFET is fully-OFF and within its "cut-off" region.

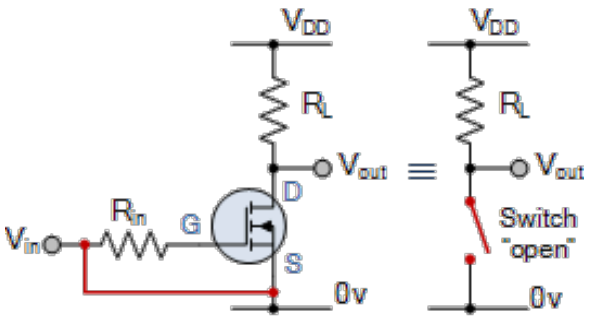


The minimum ON-state gate voltage required to ensure that the MOSFET remains fully-ON when carrying the selected drain current can be determined from the V-I transfer curves above. When V_{IN} is HIGH or equal to V_{DD}, the MOSFET Q-point moves to point A along the load line. The drain current I_D increases to its maximum value due to a reduction in the channel resistance. I_D becomes a constant value independent of V_{DD}, and is dependent only on V_{GS}. Therefore, the transistor behaves like a closed switch but the channel ON-resistance does not reduce fully to zero due to its $R_{DS(on)}$ value, but gets very small.

Likewise, when V_{IN} is LOW or reduced to zero, the MOSFET Q-point moves from point A to point B along the load line. The channel resistance is very high so the transistor acts like an open circuit and no current flows through the channel. So if the gate voltage of the MOSFET toggles between two values, HIGH and LOW the MOSFET will behave as a "single-pole single-throw" (SPST) solid state switch and this action is defined as:

1. Cut-off Region

Here the operating conditions of the transistor are zero input gate voltage (V_{IN}), zero drain current I_D and output voltage $V_{DS} = V_{DD}$. Therefore the enhancement type MOSFET is switched "Fully-OFF".

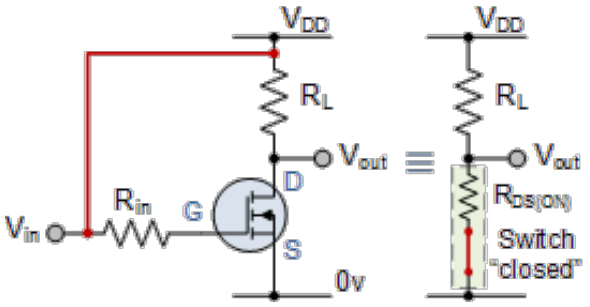


- The input and Gate are grounded (0v)
- Gate-source voltage less than threshold voltage $V_{GS} < V_{TH}$
- MOSFET is “fully-OFF” (Cut-off region)
- No Drain current flows ($I_D = 0$)
- $V_{OUT} = V_{DS} = V_{DD} = "1"$
- MOSFET operates as an “open switch”

Then we can define the “cut-off region” or “OFF mode” when using an e-MOSFET as a switch as being, gate voltage, $V_{GS} < V_{TH}$ and $I_D = 0$. For a P-channel enhancement MOSFET, the Gate potential must be more positive with respect to the Source.

2. Saturation Region

In the saturation or linear region, the transistor will be biased so that the maximum amount of gate voltage is applied to the device which results in the channel resistance $R_{DS(on)}$ being as small as possible with maximum drain current flowing through the MOSFET switch. Therefore the enhancement type MOSFET is switched “Fully-ON”.

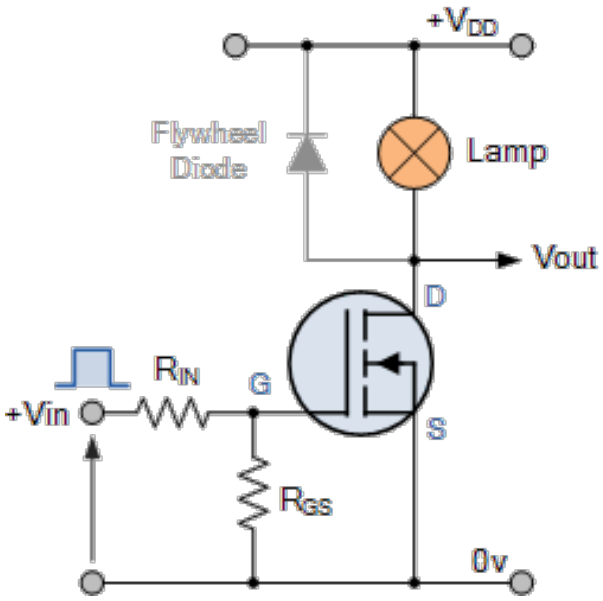


- The input and Gate are connected to V_{DD}
- Gate-source voltage is much greater than threshold voltage $V_{GS} > V_{TH}$
- MOSFET is “fully-ON” (saturation region)
- Max Drain current flows ($I_D = V_{DD} / R_L$)
- $V_{DS} = 0V$ (ideal saturation)
- $V_{OUT} = V_{DS} = \cong 0.2V$ due to $R_{DS(on)}$
- MOSFET operates as a low resistance

Then we can define the “saturation region” when using an e-MOSFET as a switch as gate-source voltage, $V_{GS} > V_{TH}$ and $I_D = Maximum$. For a P-channel enhancement MOSFET, the Gate potential must be more negative with respect to the Source.

By applying a suitable drive voltage to the gate of the FET, the resistance of the drain-source channel, $R_{DS(on)}$ can be varied from an “OFF-resistance” of many hundreds of kΩ’s, effectively an open circuit, to an “ON-resistance” of less than 1Ω, effectively a short circuit.

An example of using the MOSFET as a switch



In this circuit arrangement an N-channel eMOSFET is being used to switch a simple lamp "ON" and "OFF". The gate input voltage V_{GS} is taken to an appropriate positive voltage level to turn the device and therefore the lamp load either fully "ON" (V_{GS} = +ve), or at a zero voltage level that turns the device fully "OFF" (V_{GS} = 0).

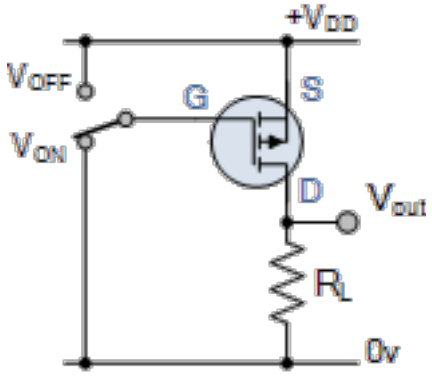
MOSFET Type	V_{GS} (+ve)	V_{GS} (0v)	V_{GS} (-ve)
N-channel Enhancement	ON	OFF	OFF
N-channel Depletion	ON	ON	OFF
P-channel Enhancement	OFF	OFF	ON
P-channel Depletion	OFF	ON	ON

Note that unlike the N-channel MOSFET whose gate terminal must be made more positive (attracting electrons) than the source to allow current to flow through the channel, the conduction through the P-channel MOSFET is due to the flow of holes. That is the gate terminal of a P-channel MOSFET must be made more negative than the source and will only stop conducting (cut-off) until the gate is more positive than the source.

Low threshold type power MOSFETs may not switch "ON" until a least 3V or 4V has been applied to its gate and if the output from the logic gate is only +5V logic it may be insufficient to fully drive the MOSFET into saturation. Using lower threshold MOSFETs designed for interfacing with TTL and CMOS logic gates that have thresholds as low as 1.5V to 2V are available.

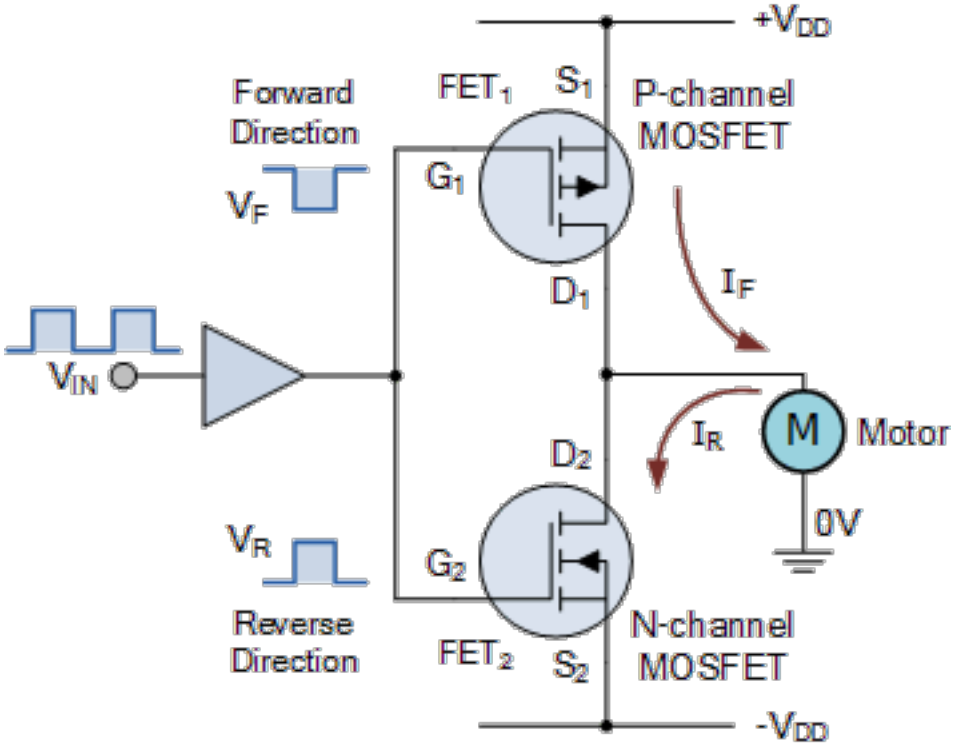
P-channel MOSFET Switch

Thus far we have looked at the N MOSFET as a switch were the MOSFET is placed between the load and the ground. This also allows for the MOSFET's gate drive or switching signal to be referenced to ground (low-side switching). But in some applications we require the use of P e-MOSFET were the load is connected directly to ground. In this instance the MOSFET switch is connected between the load and the positive supply rail (high-side switching).



In a P-channel device the conventional flow of drain current is in the negative direction so a negative gate-source voltage is applied to switch the transistor "ON". This is achieved because the P-channel MOSFET is "upside down" with its source terminal tied to the positive supply +VDD. Then when the switch goes LOW, the MOSFET turns "ON" and when the switch goes HIGH the MOSFET turns "OFF".

This upside down connection of a P-channel enhancement mode MOSFET switch allows us to connect it in series with a N-channel enhancement mode MOSFET to produce a complementary or CMOS switching device as shown across a dual supply.



The two MOSFETs are configured to produce a bi-directional switch from a dual supply with the motor connected between the common drain connection and ground reference. When the input is LOW the P-channel MOSFET is switched-ON as its gate-source junction is negatively biased so the motor rotates in one direction. Only the positive $+V_{DD}$ supply rail is used to drive the motor.

However, to avoid cross conduction with both MOSFETS conducting at the same time across the two polarities of the dual supply, fast switching devices are required to provide some time difference between them turning “OFF” and the other turning “ON”. One way to overcome this problem is to drive both MOSFETS gates separately. This then produces a third option of “STOP” to the motor when both MOSFETS are “OFF”.