SELF-ALIGNED POLYSILICON GATE METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR FOR LARGE AREA ELECTRONICS

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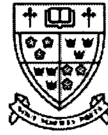

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ABSTRACT

Currently, the established large area technology is amorphous silicon where device performance is sacrificed for uniformity and low cost of fabrication. In this research, we investigate crystalline silicon technology for large area application that requires high performance devices. For example, digital X-ray tomosynthesis is one application where amorphous silicon technology cannot satisfy the requirements of low noise and real-time operation. In this work, self-aligned polysilicon gate MOSFET was developed. To achieve this goal, gate dielectric materials and gate materials were studied and a self-aligned MOSFET was developed. A mask set was designed in Cadence and devices were fabricated in the SFU IMMR fabrication facility. Characterization of the devices by C-V and I-V measurements were carried out. The results indicate that an in-house fabrication of uniform self-aligned polysilicon gate MOSFET based electronics is possible if oxide quality can be maintained.

谨以此文献给始终支持、鼓励、教育我的父母和姐姐

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CHAPTER 1 INTRODUCTION

The continuous miniaturization of microelectronics has produced increased computation power at ever decreasing cost. Despite the ubiquitous silicon chip, there is another class of electronic devices that need a large size to be useful and therefore require a different approach to fabrication. The displays and scanners that form the interface between people and the electronic world, as well as solar cells and X-ray imagers, are examples of electronic devices for which a large size is essential [1].

1.1 Motivation

In recent years, the occurrence of breast cancer has dramatically increased. Current attempts to control breast cancer concentrate on early detection by means of screening, via periodic mammography and physical examination. With current technology, some cancers become visible on mammograms only after they have been present for several years. In addition, one study has shown that about 20% of detectable cancers are overlooked or misdiagnosed on first inspection [2, 3].

Digital X-ray mammography promises to be a significant improvement over conventional mammography in the early detection of breast cancer. Digital mammography incorporates modern electronics and computers into x-ray mammography methods. Instead of acquiring an image on film, it is collected electronically and stored directly into a computer [4].

To be able to replace and improve upon current medical imaging techniques, the digital imager performance should be comparably better than conventional X-ray film technology. Mammography is one of the major applications of this area, while, it has several defects during the application in medical examination. The compression of the breast that is required during a mammography is uncomfortable. The compression also causes overlapping of the breast tissue. Mammography take only one picture, across the entire breast, in the two directions: top to bottom, and side to side. Digital tomosynthesis can eliminate the defects of conventional mammography. By creating a three-dimensional picture of the breast using X-rays, digital tomosynthesis provides a more comfortable breast screening, detects the cancer hiding within overlapping tissues, and offers views from multiple perspectives.

Crystalline silicon (c-Si) technology is adopted in our digital X-ray mammography research. The advancement in c-Si technology, together with the advantages of high density of integration, high carrier mobility, micron and sub-micron feature sizes, can allow digital X-ray mammography technology to meet tomosynthesis requirements.

1.2 Thesis Goals

In this research, we investigate c-Si technology for large area application that requires high performance devices. For example, digital X-ray tomosynthesis is one application where amorphous silicon technology cannot satisfy the requirements of low noise and real-time operation.

The goal of this work is to demonstrate a simple cost effective silicon transistor process which will form the foundation for large area c-Si imaging research at SFU. Although CMC (Canadian Microelectronics Corp.) provides MOS transistor fabrication, the cost of fabricating large area devices in CMC CMOS technology is prohibitive for research purposes.

1.3 Thesis contributions

1.3.1 MOSFET Gate dielectric materials

Gate dielectric material is essential for performance determination of MOSFET devices. In this work, the thermal furnace in SFU cleanroom facility was used to grow the SiO_2. We can get two types of SiO_2 by using different oxidation process: wet SiO_2 and dry SiO_2. C-V (Capacitance-Voltage) measurements were carried on the MOS (Metal-Oxide-Semiconductor) capacitors fabricated from the two oxides. The analysis of the C-V and breakdown curves indicates that dry oxide is suitable to serve as gate oxide in MOSFET. Wet oxide functions as field insulator between devices in this work.

1.3.2 MOSFET Gate materials

We have investigated two types of materials for MOSFET gate: crystalline/doped silicon and molybdenum. Polycrystalline silicon is the popular option for MOSFET gate for its very low metal-semiconductor work function. Molybdenum has distinct advantages to serve as gate in self-aligned MOSFET, such as high thermal and electric conductivity, high melting temperature, and the thermal expansion closely matching that of silicon.

1.3.3 SiN_x as an interlevel dielectric

SiN_x used as an interlevel dielectric in this work was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) equipment made by MVSystem®. Electrical property of SiN_x was checked by C-V and breakdown measurement.

1.3.4 Self-aligned MOSFET process design

In this work, the gate of MOSFET was used to align of the source and drain regions. This minimizes potential overlap between gate and drain/source, thus enhancing the performance of MOSFET and aids large area uniformity. Four steps were followed for self-aligned MOSFET fabrication: field oxide and gate oxide patterning, gate patterning, via holes patterning, and contact patterning. Design of the mask set was realized in Cadence® environment.

1.4 Outline of Thesis

In this research, we investigated the following topics to develop a reliable large area c-Si process:

a) a low leakage, reliable gate dielectric material,

b) a gate material with good electrical and thermal properties,

c) a low leakage, low stress, interlevel dielectric, and

d) a repeatable process, i.e., self-aligned process.

Chapter 2 explains the process for growth of the dielectrics and checks the reliability of the dielectric materials by C-V (Capacitance-Voltage) and I-V (Current-Voltage) measurements. Chapter 3 describes the design process including choice of gate

material, in perspectives of feature size, error tolerance, mask plate type and integration of the four mask layers. Detailed fabrication process is also described in Chapter 3. Measurement results from C-V and I-V measurements of the MOSFETs and test structures are presented in Chapter 4. The electronic properties of the MOSFET are analyzed based on the measurements. Chapter 5 summarizes the work done in this thesis and proposes the direction for future research.

CHAPTER 2 DIELECTRIC MATERIALS

The gate dielectric between gate and semiconductor play a critical role in the performance of a MOSFET. The properties of the gate dielectric determine the gate leakage current; therefore choosing a proper material for the gate dielectric is necessary.

2.1 Requirements for gate dielectric

Gate dielectric formation is the first thermal step in the entire process. The gate dielectric completes the capacitor formed between the gate electrode and the channel. The operating voltage and reliability of the device depend on the dielectric strength. In an ideal MOSFET, the gate dielectric performs a perfect barrier to the electron flow. Real dielectric could disrupt this ideal picture if gate voltage ramps to a high enough value or if the dielectric is too thin, which will then lead to the breakdown of the dielectric.

2.1.1 Dielectric thickness

For the MOS structure shown in Figure 2-1, the purpose is to collect as many charges as possible when a gate voltage is applied, according to the following formula:

$$Q = C_i \cdot V \qquad (2\text{-}1)$$

in which Q is the total charges that accumulate in the MOS capacitor, V is the applied gate voltage, C_i is the capacitance of the MOS structure and can be expressed by the formula below.

$$C_i = \frac{\varepsilon_0 \cdot \varepsilon_i \cdot A}{t_i} \tag{2-2}$$

where ε_0 is the permittivity of free space, $\varepsilon_0 = 8.85 \times 10^{-14} F/cm$; ε_i is dielectric constant, it is constant for a specific material; A is the area of MOS capacitor; t_i is the thickness of the dielectric material.

From Formula (2-1), large capacitance C_i is preferred for the accumulation of more charges Q under a constant V. The size of a MOSFET is limited by real device requirements, which should not be too large. Based on Formula (2-2), a large capacitance can be obtained by shrinking the thickness of the dielectric. The thinner the dielectric, the better.

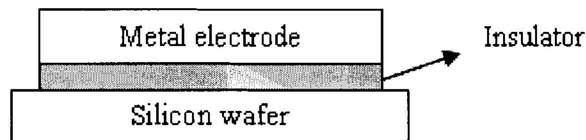


Figure 2-1 MOS capacitor.

On the other hand, a very thin dielectric tends to cause breakdown of the MOS capacitor. Preventing dielectric breakdown requires the dielectric keeping a certain thickness.

Existing literatures [5, 6] indicate that the gate dielectric tends to suffer breakdown if the MOS size goes into deep sub-micron regions. The dimensions employed in this work are in micron range and thickness is not considered to be a crucial element during the device design and fabrication.

2.1.2 Materials for gate dielectric

From formula (2-2), we can see that a material with a high dielectric coefficient (ε) is desirable for a large MOS capacitance. Silicon dioxide (SiO_2) is the conventional material for gate dielectric, with dielectric constant $\varepsilon_{ox} = 3.8$.

SiO_2 has been used as the primary gate dielectric material in field-effect devices since 1957, when the usefulness of the Si/SiO_2 material system was first demonstrated [7-13]. SiO_2 could be grown directly from the silicon substrate, which promises a good interface between Si/SiO_2 and grants it natural advantage to serve as the gate dielectric of MOSFET.

In general, the requirements for MOS gate dielectrics include:

1. High dielectric coefficient;
2. Wide band gap;
3. Ability to grow high purity, either crystalline or amorphous films on Si with a clean surface – high resistivity and breakdown voltage, low interfacial trap densities;
4. Compatibility with the substrate and the top electrode;
5. Low thermal stresses – thermal processing is necessary during the fabrication. Thermal stresses could be developed, which may change the electronic properties of the film; thus, low thermal stresses are desired;
6. Good processing capability for Si fabrication.

2.2 Growth and characterization of SiO2

2.2.1 SiO_2 growth

Thermal oxidation of silicon is easily achieved by heating the Si substrate to temperatures typically in the range of 900-1100 Degrees Celsius. The atmosphere in the furnace where oxidation takes place can either contain pure oxygen or water vapor. Both of these molecules diffuse easily through the growing SiO_2 layer at these high temperatures. Oxygen arriving at the silicon surface can then combine with silicon to form silicon dioxide. Initially, the growth of SiO_2 is only a surface reaction. However, after the SiO_2 thickness begins to build up, the arriving oxygen molecules must diffuse through the growing SiO_2 layer to get to the silicon surface in order to react.

Depending on the process environment, the reaction during oxidation could occur in one of the two ways:

$$Si + O_2 \rightarrow SiO_2 \qquad (2\text{-}3)$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \qquad (2\text{-}4)$$

The reaction process for Formula (2-3) is called dry oxidation and that for Formula (2-4) is called wet oxidation. Due to the stoichiometric relationships in these reactions and the difference between the densities of Si and SiO_2, about 46% of the silicon surface is "consumed" during oxidation. That is, for every 1 μm of SiO_2 grown, about 0.46 μm of silicon is consumed (see Figure 2-2).

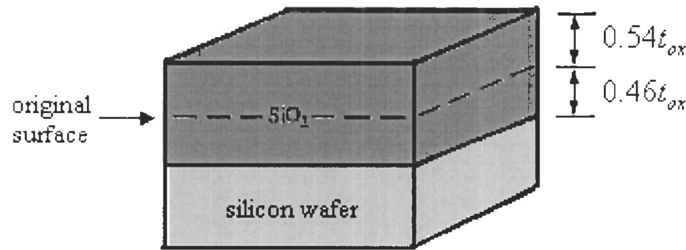


Figure 2-2 Oxidation of silicon.

Wet oxidation of silicon is typically used to rapidly grow thick oxides. SiO_2 grown by wet oxidation is inferior in quality because of the possibility of a relatively loose structure resulted by the rapid growth and is usually used as field oxide or a barrier in fabrication. On the other hand, dry oxidation of silicon is slow in growth, which leads to SiO_2 with better electrical property. Gate oxide is prepared by dry oxidation and is thinner than field oxide. Dry SiO_2 is grown and studied as gate dielectric in our work.

Before an oxidation is performed, the silicon wafer should be cleaned thoroughly to make sure there is no contamination during the process. Appendix 4 describes the whole process of RCA clean. Wafers were loaded into furnace immediately after the RCA clean was done.

The dry oxidation was carried out in 1100°C, both on p-type <100> silicon wafer and n-type <100> silicon wafer. The wafers were initially loaded into the oxidation furnace at 800°C. The temperature was then ramped up to 1100°C in nitrogen environment. The process began when the oxygen flowrate was set to 4 scfh (standard cubic feet per hour). The whole process took 165min for both n-type and p-type wafer. Then the wafers were pulled out after the temperature was cooled down to 800°C.

To improve the quality of dry oxide, a thorough furnace clean was carried out after the growth of the first oxide. Dry oxides were grown on p-type and n-type wafer again after the furnace clean had been completed. The oxides grew before and after furnace clean were both analyzed by C-V measurements. We name the oxide grown before furnace clean as “first oxide”, the oxide grew after furnace clean as “second oxide”.

Thicknesses of the dry oxides were measured by both Tyger® Thin Film Analyzer and Tencor® Profilometer. There were small differences between the thicknesses obtained from these two methods, which indicate statistical error or the possibly uneven surface of the oxide. Thicknesses of the first and second dry oxide on p-type and n-type wafer are listed in Table 2-1, respectively. DEV stands for “analyzer deviation” in the table.

Table 2-1 Thicknesses of dry oxide (first and second oxide).

	n-type wafer (Å)		p-type wafer (Å)	
	by Tyger® Thin Film Analyzer	by Profilometer	By Tyger® Thin Film Analyzer	by Profilometer
First oxide	1869 (DEV: 38)	1950	1925 (DEV: 36)	1993
Second oxide	1934 (DEV: 3)	2011	1961 (DEV: 22)	2056

2.2.2 SiO_2 characterization

Capacitance-Voltage measurement and breakdown test were performed to characterize the thermally grown dry oxide.

2.2.2.1 C-V measurement for SiO2

To facilitate the C-V measurement, a layer of 0.5μm aluminum was sputtered on the surface of dry oxide. The wafers were then patterned in squares, as shown in Figure 2-3. The sides of the squares are 0.5, 1, 1.3 mm, referred to as C_0, C_1 and C_2.

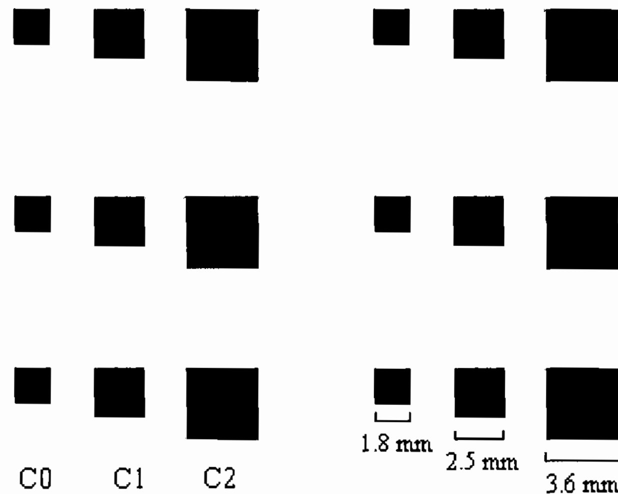


Figure 2-3 Patterned MOS capacitance structures.

The C-V measurement on SiO_2 was done on the Keithley 590 CV Analyzer, which is controlled by computer through GPIB (General Purpose Interface Bus). The C-V curve for $0.5 \times 0.5 mm^2$ dimension MOS capacitor of the first dry oxide p-type wafer is shown in Figure 2-4.

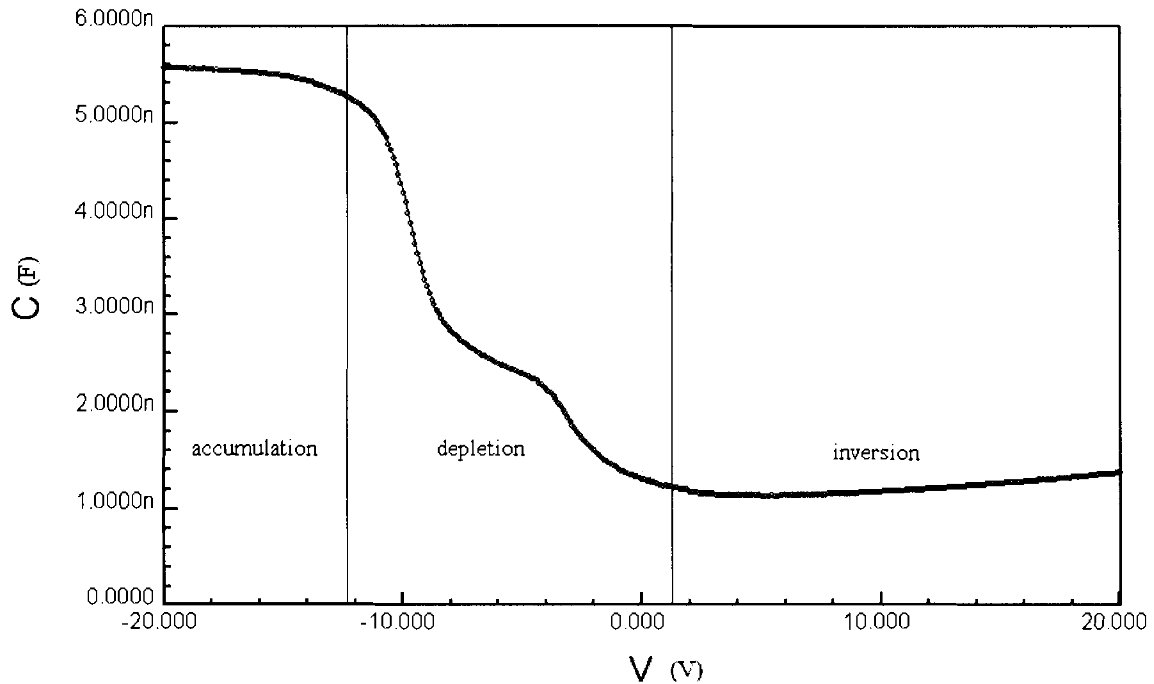


Figure 2-4 C-V curve for $0.5 \times 0.5 mm^2$ **imension MOS capacitor (first dry oxide on p-wafer).**

From the C-V curve above, we can see that shape of the curve is consistent with standard C-V curve, except for a single bump. The measured values of the capacitances also agreed with the calculated values.

As emission time constants of interface traps depend on the energy difference between the surface state energy, E_{it} , and the band edges, only negative charged interface states between the conduction band and a limiting energy state $E_{\lim}$, (about 0.8eV – 1eV from the conduction band edge) are able to emit electrons when sweeping from inversion to accumulation, because in this range emission time constants are short.

The remaining negatively filled surface states can only be discharged by capturing holes when the surface hole concentration becomes high enough. This is detected by a change in the slope of C-V curve. Within a narrow range of surface potential between the

two points of the bump, most of the negatively charged surface states can be discharged by hole capture. The width of the bump depends on the negatively charged surface state density in non-equilibrium, i.e., filled surface states, which can neither be discharged by emission processes due to long emission time constants, nor by capture processes due to low majority generation in depletion [14]. The band diagram of this phenomenon is shown in Figure 2-5.

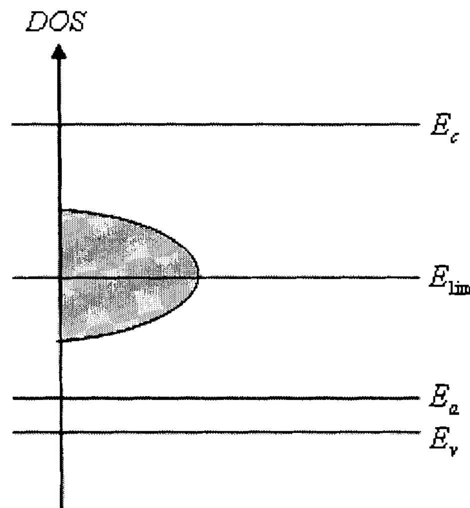


Figure 2-5 Band diagram of C-V bump.

The bump in the CV characteristics suggests trap states centered within the bandgap, as opposed to the disorder induced tails of states that extend from the band edges. Acceptor energy level E_a determines the point on the C-V at which the bump occurs.

The second dry oxides prepared in a clean furnace tube show better properties than the first ones. Figure 2-6 depicts the C-V curve for C_0 MOS capacitor of the second dry oxide p-type wafer.

We can see from the C-V curve for the second time dry oxide that the curve shows a smoother slope, and the bump has been eliminated.

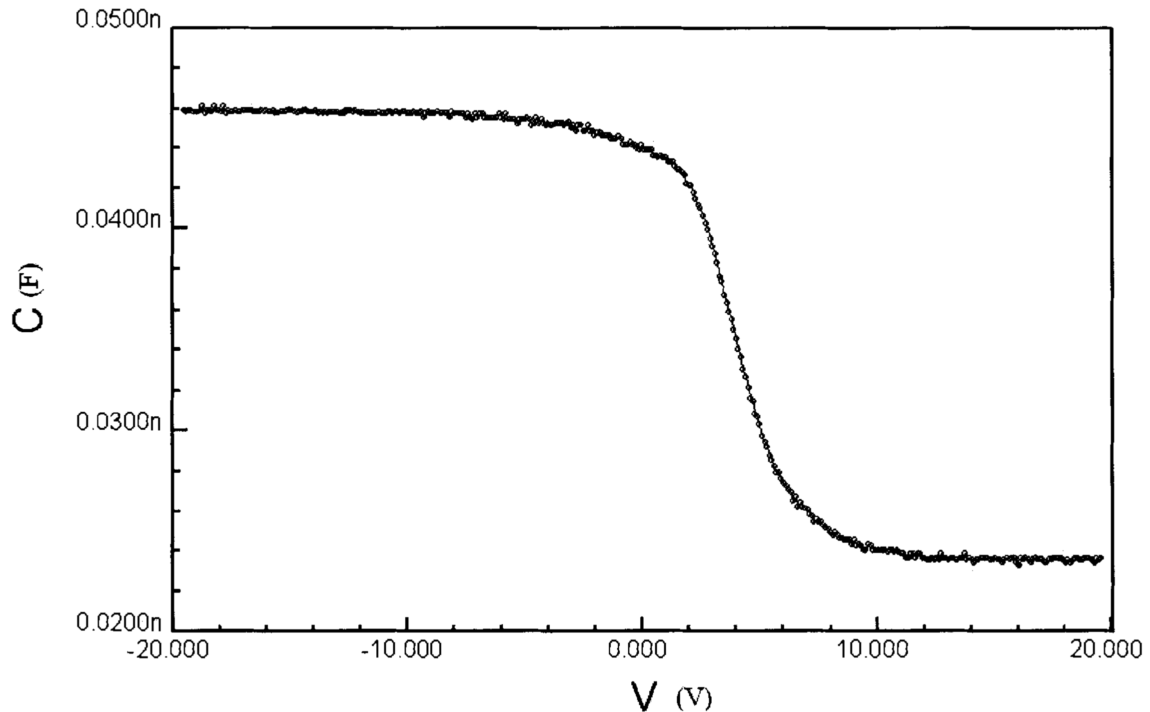


Figure 2-6 C-V curve for C_0 MOS capacitor (second time dry oxide on p-wafer).

MOS capacitances can be calculated from Formula (2-2) or extracted from C-V curves. Table 2-2 compares the two sets of values on both p-type and n-type wafers, the thickness obtained from the values measured by Tyger® Thin Film Analyzer.

On comparing the two sets of capacitances, we can conclude that the deviation between measured value and calculated value increases when the capacitor dimension increases. The error might stem from the structure of the MOS capacitor. During fabrication, we only etched the top electrode of the capacitor, left the oxide layer unpatterned, which can be shown in Figure 2-7.

Table 2-2 Comparison of tested and calculation values for SiO_2 MOS capacitors.

	p-type wafer (nF)		n-type wafer (nF)	
	Tested value	Calculated value	Tested value	Calculated value
C2	0.197	0.255	0.217	0.252
C1	0.1375	0.151	0.147	0.148
C0	0.045	0.03775	0.0469	0.0372

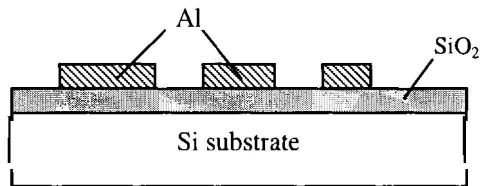


Figure 2-7 Pattern structures of MOS capacitors.

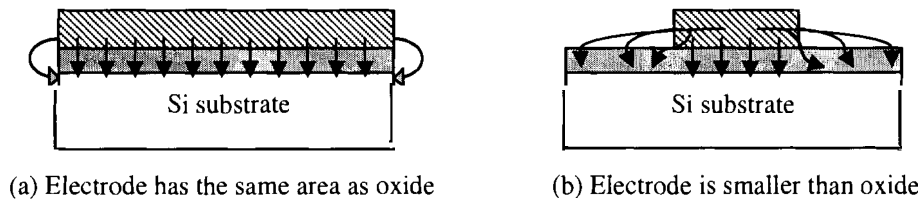


Figure 2-8 Fringing field in different patterned MOS structure.

When the Al electrode area is smaller than the oxide layer area, fringing field could be generated [15], as shown in Figure 2-8, that would lead to an influence on the measured values of capacitors. As the electrode area increases, more fringing fields will be generated. This is the reason that MOS capacitor with larger electrode area intends to

have larger deviation between measured and calculation capacitance than capacitor with smaller electrode area.

2.2.2.2 SiO_2 breakdown test

We have assumed that oxide is a perfect insulator. If a high voltage is applied on the oxide, breakdown can occur, which can lead to a device failure. Dielectric breakdown in insulators is a phenomenon that limits the operation of many electrical components [16].

The purpose of breakdown test on dielectric materials is to test its property on the application of high voltages with a gate oxide of about 200nm. The breakdown field for SiO_2 is normally $6\,MV/cm$.

A breakdown test was performed on the MOS capacitors used for C-V measurement using an Agilent 4156C Semiconductor Analyzer, which was controlled by computer through GPIB connection.

Figure 2-9 describes the property of current versus voltage for $1.3\times1.3mm^2$ dimension MOS capacitor on p-type wafer. The voltage sweeps from 0V to 100V. It can be seen that the current is almost zero before the voltage reaches 20V. After voltage exceeds 20V, the current begins to increase with voltage. When the voltage reaches 92V, the current increases exponentially and breakdown occurs.

The dry oxide was grown in the cleaned thermal furnace tube. From Figure 2-9, and the obtained thickness of dry oxide 200nm, the breakdown field for our dry oxide is evaluated to $4.6\,MV/cm$. This breakdown field is in the reasonable range of breakdown field, indicating that the property of the dry oxide is acceptable.

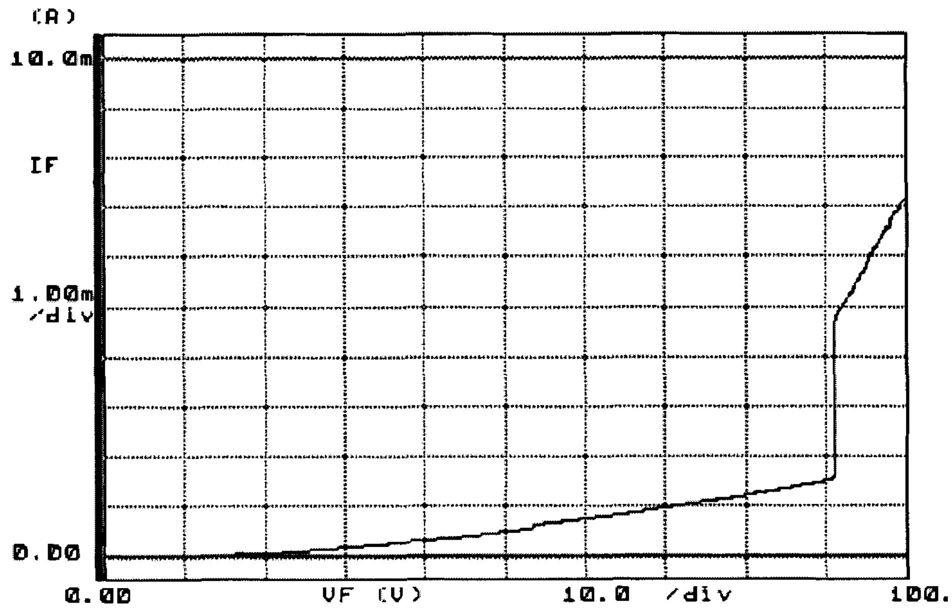


Figure 2-9 Breakdown curve for C_5 MOS capacitor (second dry oxide on p-type wafer).

2.3 Growth and characterization of SiN_x

2.3.1 SiN_x growth

In this work, besides SiO_2, SiN_x was also grown and characterized. SiN_x was used as an interlevel dielectric and was prepared by PECVD.

PECVD is a process in which one or more gaseous reactants are used to form a solid insulating or conducting layer on the surface of a wafer. This process is enhanced by the use of a vapor containing electrically charged particles or plasma at lower temperatures [17]. Figure 2-10 briefly explains the PECVD process in our cleanroom.

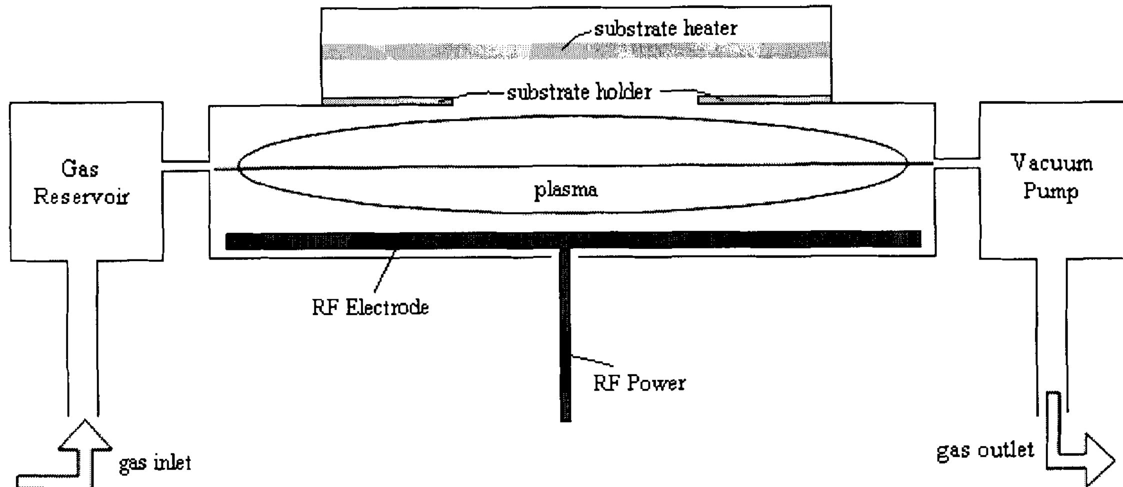


Figure 2-10 Scheme of PECVD.

Table 2-3 Parameters of low power PECVD SiN_x.

Temperature		150 °C
Pressure		500 mTorr
Deposition Time		45 min
RF power		1 W
Flowrate	SiH_4	2.7 sccm
	NH_3	150 sccm
	H_2	100 sccm

2.3.2 SiN_x characterization

2.3.2.1 C-V measurement for SiN_x

C-V measurements for SiN_x were also completed on Keithley 590 CV Analyzer. Figure 2-11 below shows the C-V curve of C_1 MOS structure on n-type wafer.

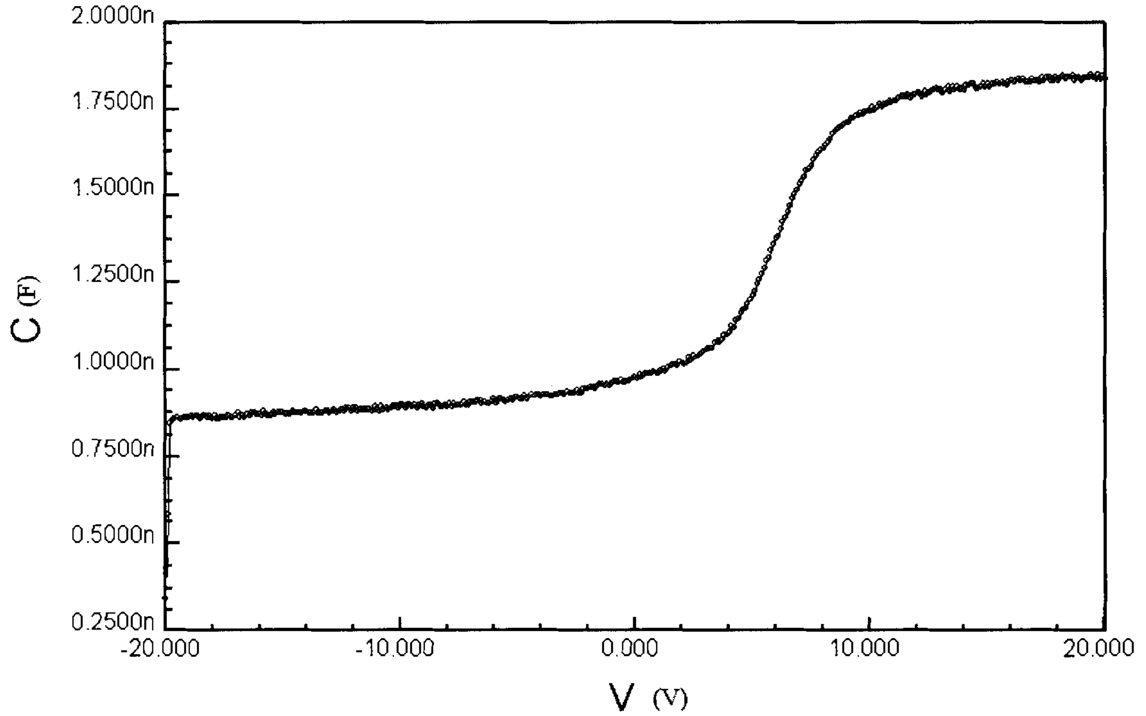


Figure 2-11 C-V curve for C_1 MOS capacitor (low power SiN_x on n-type wafer)

Table 2-4 Comparison of tested and calculated values for SiN_x MOS capacitors.

	n-type wafer (nF)	
	Tested value	Calculated value
C2	2.91	2.96
C1	1.73	1.75
C0	0.401	0.438

From the Figure 2-11, the C-V curve for our low power SiN_x is consistent with a normal MOS C-V curve. The curve bump that existed on the oxide C-V curve did not occur for the SiN_x C-V curve. Table 2-4 compares the calculated and tested values of

SiN_x MOS capacitors. Thickness of the SiN_x is 400nm, which was measured by Tyger® Thin Film Analyzer.

2.3.2.2 Breakdown test for SiN_x

The breakdown test on SiN_x film was implemented on Agilent 4156C Semiconductor Analyzer. The breakdown field for SiN_x is normally $6\,MV/cm$.

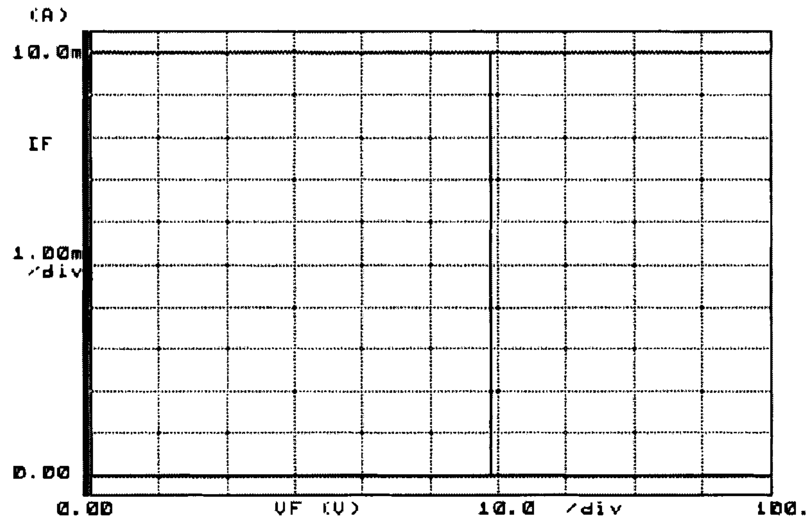


Figure 2-12 Breakdown test curve for C_1 MOS capacitor (low power SiN_x on p-type wafer).

Figure 2-12 shows the breakdown curve for the SiN_x. The current remains almost zero before it reaches 59V, at which point the breakdown occurs. The breakdown field for the SiN_x film is $3\,MV/cm$. This value differs from the standard SiN_x breakdown field $6\,MV/cm$.

It is important to note that the SiN_x film is not optimized. However, it appears to be adequate as an interlevel dielectric from its C-V and breakdown characterization.

CHAPTER 3 SELF ALIGNED MOSFET

3.1 Fabrication process for self-aligned MOSFET

3.1.1 Self-aligned MOSFET

Defining and doping Source and Drain area is the crucial step during the fabrication of MOSFET. Conventional technique for this step is doping by diffusion or ion implantation, and then building up gate on top of the active area [18]. When building gate after D/S area doping, there should be no overlap between Gate/Drain and Gate/Source. But in fabrication, overlap is inevitable and necessary for this technique. As we know, the Gate should cover all the length of the channel, otherwise, the inversion layer under Gate will not connect the Drain and Source together and a conducting channel will never exist. For this case, the device could not work any more. We call this "broken channel" in this work. Figure 3-1 depicts phenomenon of the capacitance parasitics occurred in the conventional MOSFET.

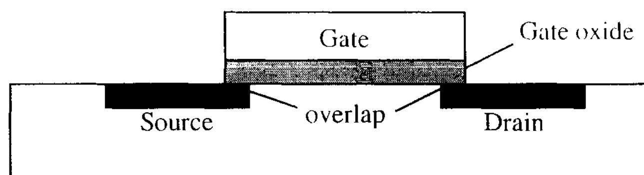


Figure 3-1 Phenomenon of capacitor parasitics in MOSFET.

Misalignment during fabrication is hard to avoid. If the gate length is designed exactly as long as the channel and when misalignment occurs, the possibility of broken channel increases dramatically. To prevent this, the length of the Gate is always slightly

longer than the channel in design. But the substantial parasitic capacitances that result from the gate electrode overlapping both the drain and the source will seriously degrade the high frequency characteristics of individual devices and result in slower circuit speeds [19].

Self-aligned MOSFET structure could solve this problem and yield uniform devices over a large area. The idea of self-aligned MOSFET is by using a pre-defined Gate as the mask for the step of doping.

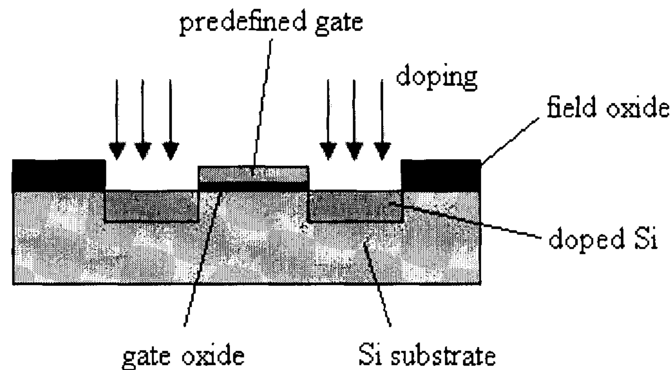


Figure 3-2 Idea of self-aligned MOSFET.

As shown in Figure 3-2, the potential overlap between G/D and G/S could be eliminated by the predefined Gate during doping process.

The challenge for self-aligned structure is the Gate material. Following the principle idea of self-aligned structure, Gate is formed before Source/Drain doping. There are two doping techniques, diffusion and ion implantation. Diffusion requires a temperature as high as 1000°C in diffusion furnace. Although ion implantation could be performed under relatively low temperature (~200°C), the crystal damage caused by the high-energy ions must be annealed at high temperature (~800°C). As the traditional Gate

material, aluminum will diffuse into gate oxide when the temperature exceeds 500°C. Another Gate material is thus needed for the implementation of a self-aligned MOSFET.

3.1.2 Requirements for gate materials in self-aligned MOSFET

To serve as the gate for self-aligned MOSFET, the candidate material should possess the following properties:

- High melting point to withstand the high temperature during the diffusion
- Stable at high temperature and thermal expansion coefficient similar to silicon
- Good compatibility with the gate dielectric material, in this work, SiO_2
- Should prevent diffusion into the gate oxide and do not react with gate oxide
- Good electrical and thermal conductivity

Doped polycrystalline silicon (poly-Si) and molybdenum were the two candidates investigated in this work. Doped poly-silicon was found to be a very convenient gate material since it withstands the high anneal temperature and can be oxidized just like silicon. An acceptable electrical conductivity could also be obtained from doped poly-silicon.

Molybdenum is another good gate candidate that is suitable for self-aligned process. Its self-aligning gate feature, high melting temperature, high electrical and thermal conductivity and good match of thermal expansion with silicon make it an ideal material for use in digital ICs. For the different gate material, the fabrication process

needs to be adjusted accordingly. The following sections give the fabrication processes for molybdenum gate and poly-silicon gate self-aligned MOSFETs.

3.1.3 Fabrication process for molybdenum gate self-aligned MOSFET

Figure 3-3 describes the fabrication process of molybdenum gate self-aligned MOSFET.

3.1.4 Fabrication process for silicon gate self-aligned MOSFET

In our process, when using silicon as the gate for MOSFET, the silicon is initially in the amorphous state. It could be doped during PECVD deposition, or during the Source/Drain diffusion. Because the temperature for diffusion is set to 1000°C for 40 min and there is an additional drive-in process for diffusion at 1000°C for 30 min, the amorphous silicon is crystallized during the period in high temperature furnace.

For silicon gate process, the difference occurs during the silicon gate patterning. KOH solution is used to pattern amorphous silicon, which also attacks the positive photoresist that protects the desired area.

This problem is solved by growing a layer of SiN_x on top of the amorphous silicon layer. The SiN_x layer is patterned first by the photoresist. Because SiN_x can stand well in KOH solution, it performs as mask to protect silicon during silicon patterning. An additional layer of SiN_x requires several more treatment during the fabrication process.

Figure 3-4 describes the process for silicon gate self-aligned MOSFET. Table 3-1 summaries the steps required by the two processes.

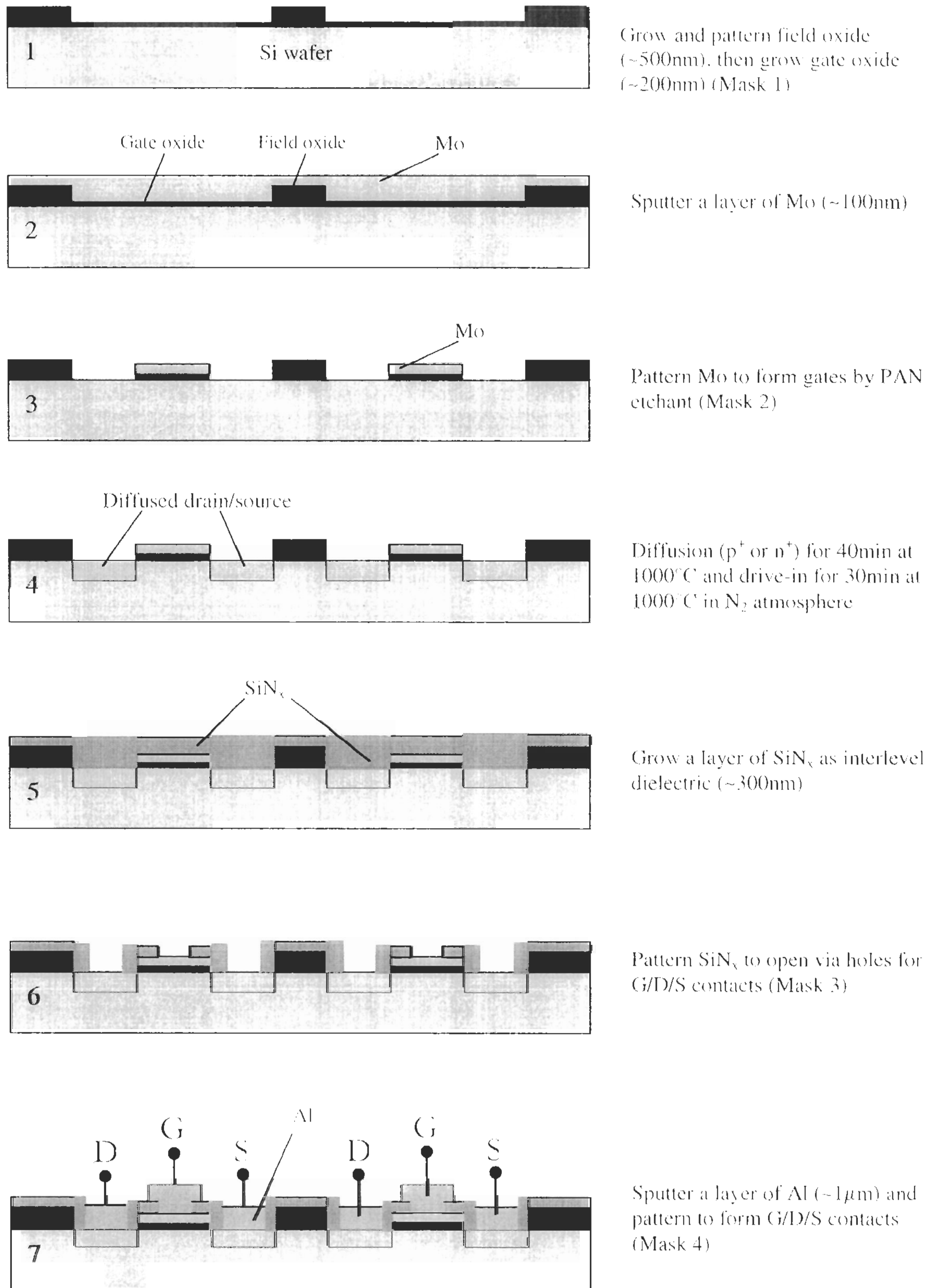


Figure 3-3 Process steps of molybdenum gate self-aligned MOSFET.

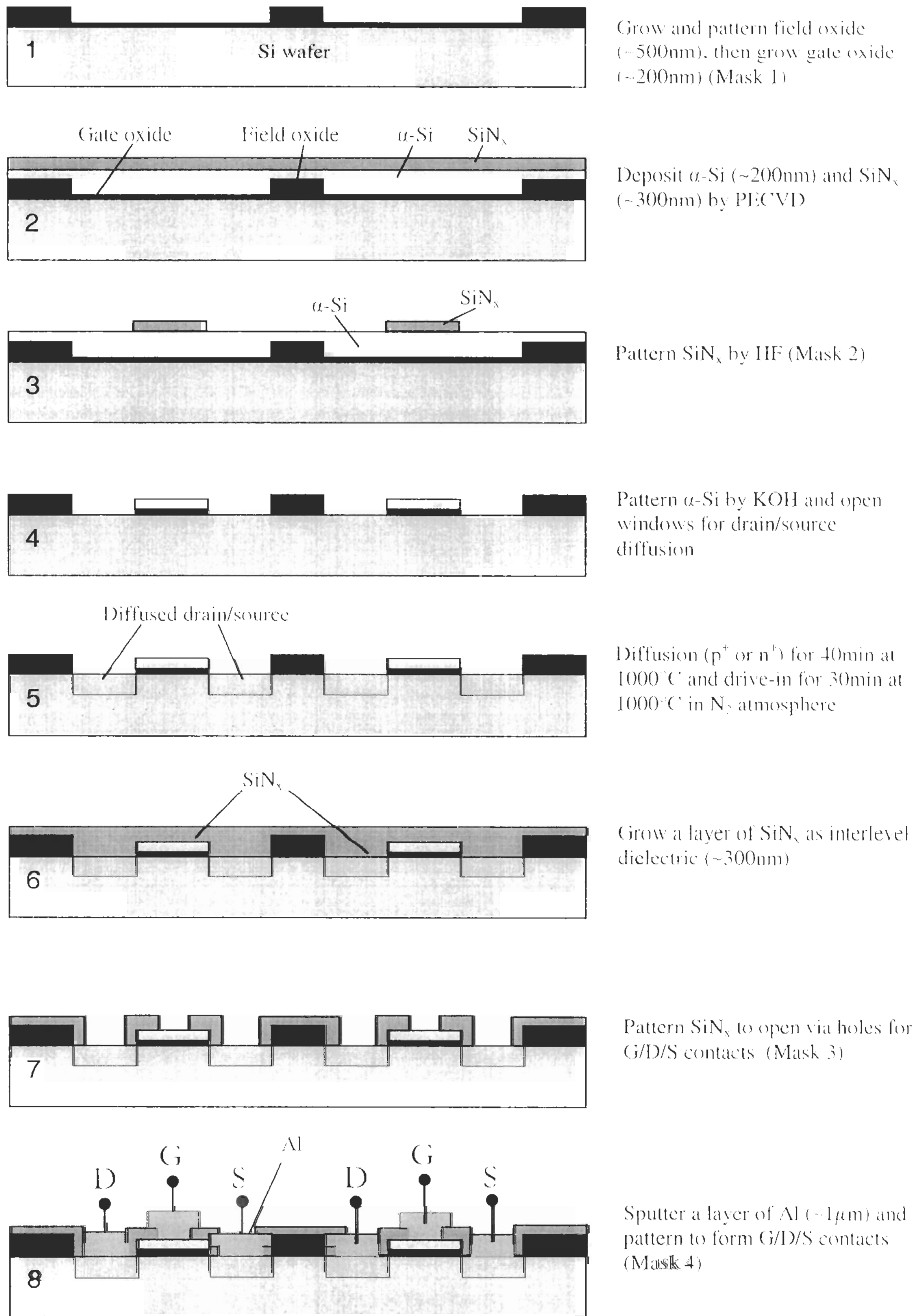


Figure 3-4 Process steps for Si gate self-aligned MOSFET.

Table 3-1 Summary of Mo-gate and Si-gate process.

	Mo-gate process	Si-gate process
Oxidation	2	2
Diffusion	1	1
PECVD	1 (SiN_x)	2 (SiN_x and a-Si)
Metal sputtering	2 (Mo and Al)	1 (Al)
Photolithography	4	4

3.2 Mask design for self-aligned MOSFET

Although difference exists between the fabrication processes for Mo gate and Si gate, requirement of masks for these two processes is the same. There are four masks needed in total during the whole fabrication process, which are for the steps of field oxide patterning, gate material (Mo or Si) patterning, via holes opening and G/D/S electrodes patterning.

3.2.1 Mask design rules

There are two types of photoresist: positive and negative. A positive photoresist responds to UV light in such a way as to make the exposed regions soluble and a positive image is thereby stored. A negative photoresist acts in the opposite way.

Positive photoresist MICROPOSIT® S1813® was used in this work. Based on the fabrication process described in previous sections with consideration of the positive photoresist, the four masks employed in the process could be as followings:

- Mask 1 Dark field (to create the active windows)
- Mask 2 Clear field (to form molybdenum or silicon gate)

- Mask 3 Dark field (to open the contact holes)
- Mask 4 Clear field (to form aluminum contact)

The minimum feature size of a technology is typically denoted by the narrowest width of a wire that it can produce. Design rules are developed for each separate fabrication sequence. Essentially, the rules contain the minimum feature size, and more important, the minimum overlap between two mask layers to ensure that the two features will be coincident when fabricated. Suitable gaps between features are also stated in the rules to ensure the features should not touch each other when fabricated. Design rules depend upon the expected alignment error that will be introduced during fabrication [20].

Masks for self-aligned MOSFET in this work are designed in CAD (Computer Aided Design) tool with the name of Cadence®. Cadence always comes with DRC (Design Rule Checker) for different fabrication technique (e.g. $0.35\mu m$ or $0.18\mu m$), which could automatically check the design against the rules. While, in this work, the minimum feature is $10\mu m$ and much larger than the range of DRC, which means it requires the designer to follow the rules during designing and manually check the design after it is done.

There are 4 design layers in total for self-aligned MOSFET; usually it needs 4 different mask plates for fabrication. The idea of 4-in-1 mask is to integrate 4 different layer designs into a single mask plate, on which a layer occupies a quarter of the plate. Figure 3-5 explains the idea for the 4-in-1 self-aligned MOSFET mask design. In the figure, each quarter was splitted into 9 parts and one part was called one die in this work. The arrows in the four quarters indicate the direction of the structure in each quarter. After the alignment of the first layer, user can rotate the mask 90 degrees clockwise and

the second layer will be in the right position to be aligned. It is the same when aligning the third and fourth layers. By this means, the mask plates are saved by sacrificing the available area on the wafer.

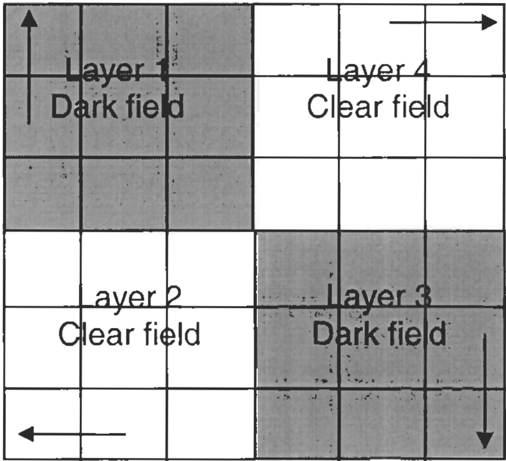


Figure 3-5 Illustration of 4-in-1 self-aligned MOSFET mask set (arrows are the directions of the structures in each quarter).

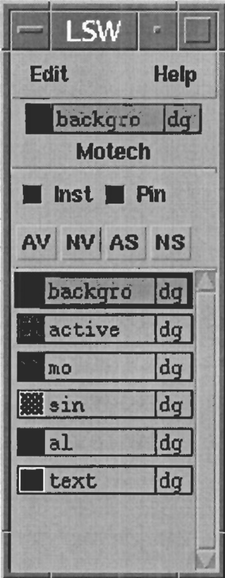


Figure 3-6 Layers definition in Cadence.

The design rules for self-aligned MOSFET are stated below.

1. Layers in the designing environment (from bottom to top, shown in Figure 3-6): background, active, mo (gate layer), sin (passivation layer), al (top pad), text (technology file is given in Appendix 3)
2. Feature size: $10\mu m$;
3. Minimum overlap: $2\mu m$;
4. Minimum bond-pad dimension: $150\times150\mu m^2$.

3.2.2 Structures on masks

The basic structures on mask are composed of MOSFETs, APS & PPS pixels and arrays, capacitors, diodes, continuity test structures and TLM (Transfer Length Method).

MOSFET

To test the effect of different gate length L on the MOSFET, a series of gate lengths, from 20μm to 1280μm in order of double increases, were employed during the design. For a fixed gate length, the width of active area, which determines the gate width W, also step increases from 20μm to 1280μm. Figure 3-7 shows the MOSFET array when gate length $L = 20\mu m$.

APS & PPS pixel and arrays

Figure 3-8 explains the circuit schematic for a single PPS pixel and the application in PPS array. PPS pixel is composed of a transistor and a photodiode. Figure 3-9 describes an APS pixel circuit schematic and the corresponding pixel layout. APS pixel consists of four transistors and a photodiode (not shown in the figure). APS and PPS pixel will be studied in future work.

Capacitors and diodes

Capacitors can be used to test the property of gate oxide, which directly determines the performance of MOSFET. Diodes may be employed by PPS and APS pixel, test of a single diode could help to analyze the performance of a circuit pixel.

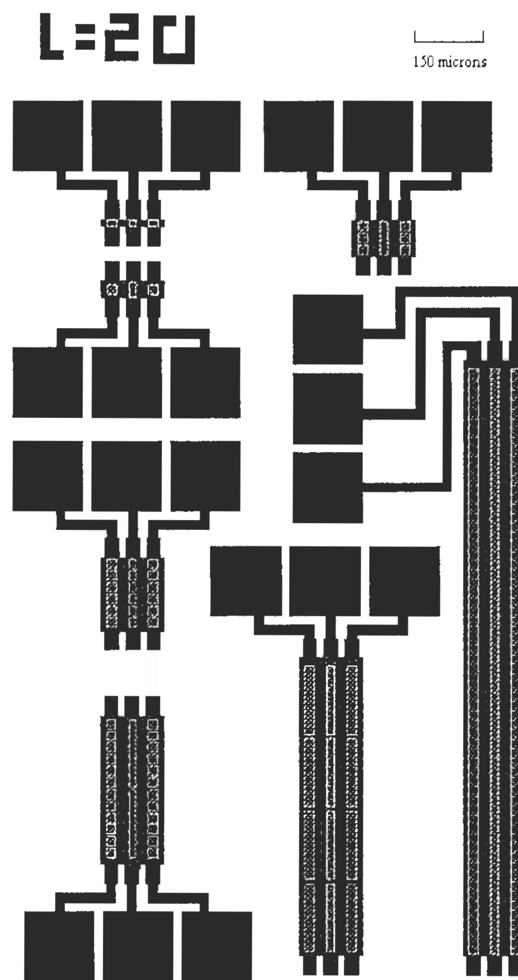


Figure 3-7 MOSFET test structures (L=20, W= 20, 40, 80, 160, 320, 640 and 1280). unit: μm.

TLM

TLM (Transfer Length Method) test structure, proposed originally by Shockley [5], was used to determine both the contact resistance R_c and sheet resistance R_s of silicon film in this study. Figure 3-8 describes the idea of TLM.

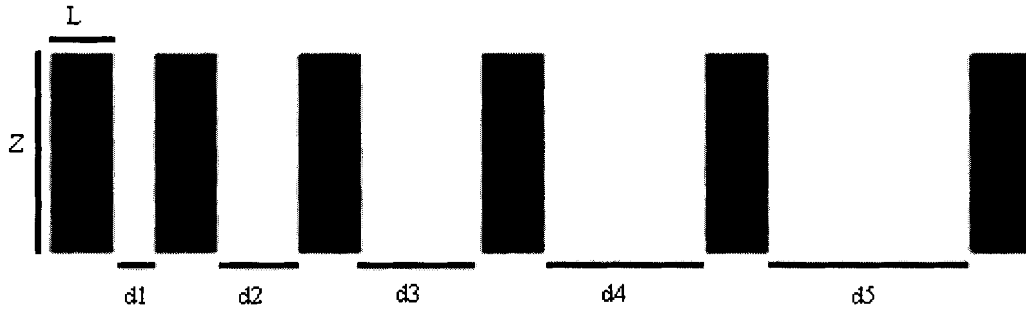


Figure 3-8 A transfer length method test structure.

A current-voltage (I-V) measurement will be taken to measure the resistance R_T between two neighboring pads by applying a series of voltage. The components for R_T can be expressed by the formula below.

$$R_T = R_s + 2R_c \tag{3-1}$$

In which, R_c is contact resistance and R_s is sheet resistance.

Through this way five different R_T will be measured for the five different distances in the structures. Figure 3-9 is the plot of R_T versus distance d, which is linear and has intercepts with x- and y-axis.

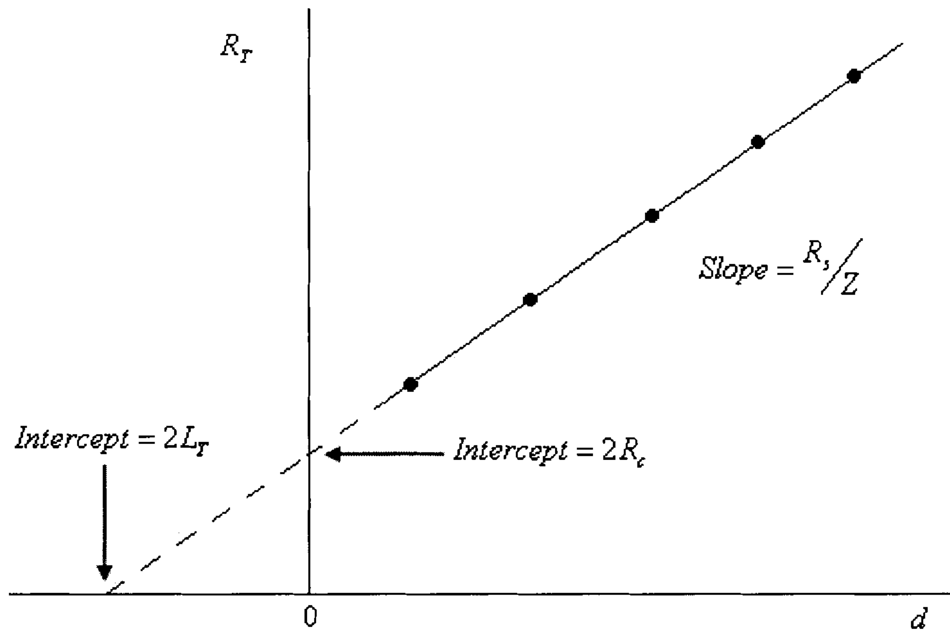


Figure 3-9 Total resistance as a function of contact spacing in TLM test structure.

In the plot, L_T is the so-called transfer length, the distance required for current to flow into or out of the ohmic contact. From the plot, the slope leads to the sheet resistance R_s with the contact width Z independently measured. The intercept at $d = 0$ is $R_T = 2R_c$ giving the contact resistance. The transfer length method gives a complete characterization of the contact by providing the sheet resistance and the contact resistance [5].

Continuity/Isolation test structure

Due to the error tolerance of fabrication process, unwanted short or open structures might exist if improperly designed. Probable explanations include incomplete etching, overetch or material breakage. Purpose of the continuity/isolation structure test structure is to test the reliability and possible minimum structure of the cleanroom fabrication process. During the design, the width of wire and the distance between wires

could be the basic variables to test the process tolerance. Figure 3-10 and 3-11 show the typical defects during fabrication process and the continuity/isolation structures of the mask design in this work.

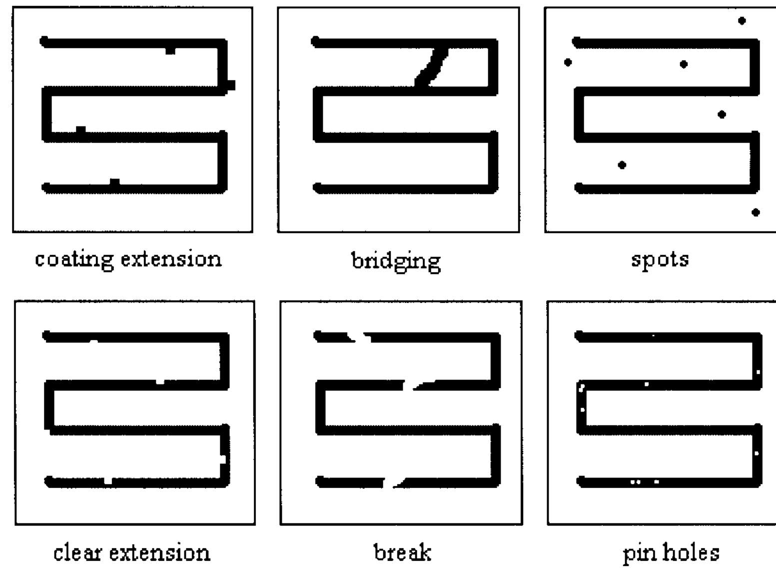


Figure 3-10 Typical defects during fabrication process.

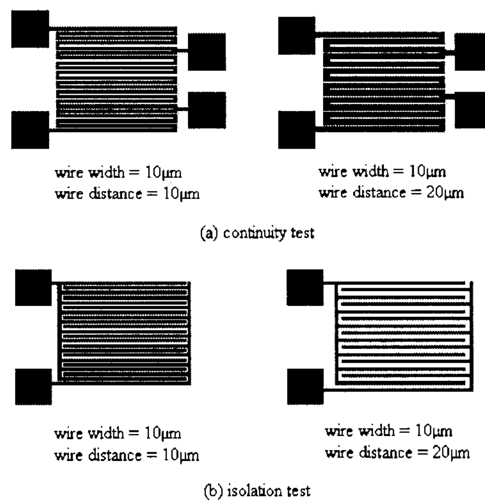


Figure 3-11 Continuity/Isolation test structures used in this work.

3.2.3 Formation of 4-in-1 mask

As shown in Figure 3-5, each quarter of the wafer was split into 9 parts and one part was called one die. Figure 3-12 shows one die on the mask in this work.

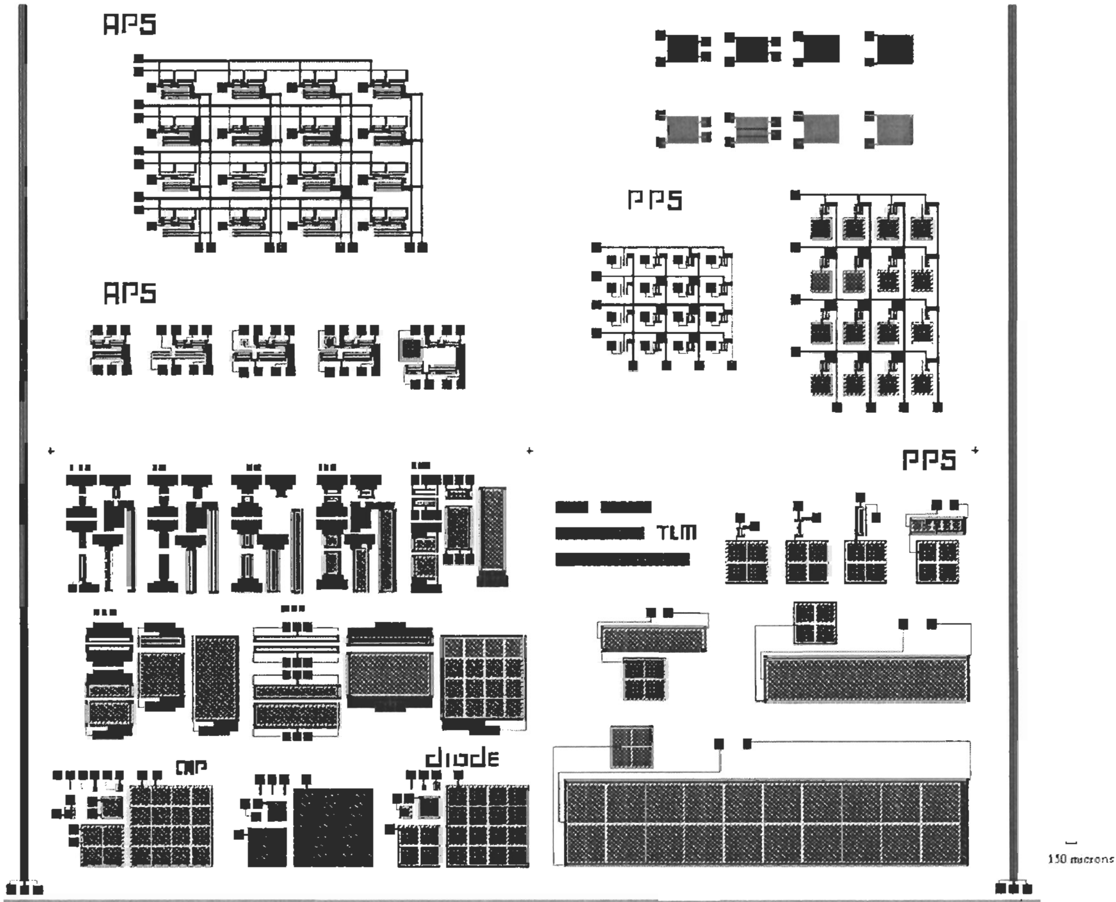


Figure 3-12 Layout of a single die.

3.3 Fabrication Process

3.3.1 Field/gate oxide growth

In this work, wet oxidation was used for field oxide growth and dry oxidation for gate oxide. The relations between temperature and time for wet/dry oxidation are based on the growth charts [21].

The desired thickness for wet oxide and dry oxide are 500nm and 200nm, respectively. Temperature for the thermal oxidation is set at 1100°C. Table 3-2 depicts the parameters used during the wet/dry oxidation.

Table 3-2 Parameters for wet/dry oxidation.

	Wet oxidation	**Dry oxidation**
Thickness desired	500 nm	200 nm
Temperature	1100°C	1100°C
Time needed	50 min	145 min
O_2 flowrate	———	4 scfh
N_2 flowrate	4 scfh	———
Thickness grown	430 nm	170 nm

The actual oxide thickness is measured both by Tyger® Thin Film Analyzer after growth and Tencor® Profilometer during later fabrication steps. We can see the thickness is in an acceptable range to be used in device fabrication.

Mask 1 is used to pattern the field oxide. MICROPOSIT® S1813 photoresist and MICROPOSIT® MF-319 developer were used during the alignment and development process. Figure 3-13 describes the process flow and the windows opened for dry oxidation. Figure 3-14 shows the opened window in field oxide for the growth of gate oxide.

Experimental etch rate is 120 nm/min and 75 nm/min for wet oxide and dry oxide, respectively.

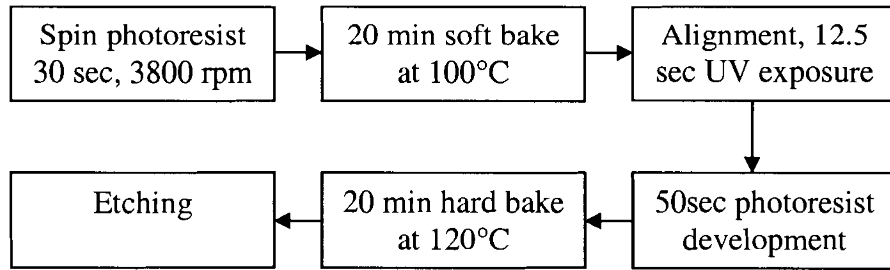


Figure 3-13 Flowchart for mask alignment and development.

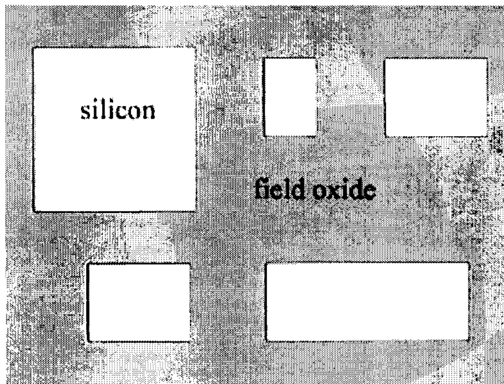


Figure 3-14 Opened windows for dry oxidation.

3.3.2 Gate material pattern and self-aligned diffusion

Two types of gate materials were used in this study — molybdenum and silicon. For the different fabrication processes of these two gate materials, the growth and pattern of them were discussed separately.

3.3.2.1 Molybdenum gate pattern

The basic features of molybdenum (Mo) are its high melting temperature, good match of thermal expansion with silicon and high electrical and thermal conductivity. To serve as gate of MOSFET, Mo not only reduces the threshold voltage, but also improves the speed of MOS devices. With its high melting temperature, Mo is suitable to be employed as gate material for self-aligned MOSFET.

100nm-thick molybdenum is deposited on the wafer by sputtering. Patterning Mo to form the device gates and expose drain/source area is achieved by the Mo etchant (PAN). PAN is the abbreviation for the three components of the solution — Phosphoric acid, Acetic acid and Nitric acid. The three acids are mixed together with water according to the following recipe [22]:

456 ml Phosphoric acid (H_3PO_4)

36 ml Acetic acid (CH_3COOH)

18 ml Nitric acid (HNO_3)

90 ml DI water

Mo coated wafers are stirred in this solution until the unprotected Mo is completely removed. For the best etching result, the solution was heated and kept at 50°C. The etching rate for Mo in PAN solution at 50°C is approximately 100Å/sec.

3.3.2.2 Solid-solid diffusion process

The diffusion process can be grouped into two categories: p-type (boron) diffusion and n-type (phosphorous) diffusion [23]. The p- or n-well region is defined by the pre-defined gate to form self-aligned doped drain/source. The surface concentration during such a solid source diffusion is usually limited by the solid solubility of the dopant in silicon.

Boron diffusion

Source for boron diffusion (p^+ diffusion) is a ceramic wafer of boron nitride (BN), which has been oxidized at 1000°C, 25% oxygen atmosphere, resulting in a surface layer of B_2O_3 glass. During the diffusion, this glass slowly evaporates from the BN wafer and

deposits on the silicon wafer. The thin layer of B_2O_3 provides elemental boron for the deposition into the silicon via the reaction [21]:

$$2B_2O_3 + 3Si \rightarrow 4B + 3SiO_2 \quad (3\text{-}2)$$

This is the so-called "infinite-source diffusion" step because the source is always there during the deposition.

After the desired amount of boron is deposited on the silicon wafer, the BN source is removed, and the boron is diffused deeper into the silicon wafer during a high-temperature limited-source diffusion (or "drive-in") step.

Phosphorous diffusion

The process for phosphorous diffusion (n^+ diffusion) is similar to the boron diffusion, except the source for phosphorous diffusion is a ceramic wafer of SiP_2O_7. P_2O_5 is generated according to the following reaction:

$$SiP_2O_7 \rightarrow SiO_2 + P_2O_5 \quad (3\text{-}3)$$

The thin layer of P_2O_5 provides elemental phosphorus for the diffusion into the silicon via the reaction [21]:

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \quad (3\text{-}4)$$

From experiments, the Mo gate was destroyed completely after diffusion process. One possible explanation for the destruction of Mo gate is due to the stresses accumulated in the thin film during the high temperature diffusion process. The temperature of diffusion was 1000°C for 1 hour and the resulting wafer had its Mo gates peeled off.

3.3.2.3 Silicon gate pattern and D/S windows opening

As stated in previous section, the fabrication process will be modified if the gate material switches to silicon. Because the KOH etchant used for silicon patterning attacks the photoresist, an additional layer of SiN_x is needed to protect silicon during the etching process.

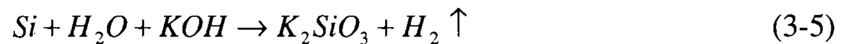
Table 3-3 Parameters for amorphous Si and SiN_x PECVD deposition.

		Amorphous silicon			SiN_x
		intrinsic	n^+	p^+	
Flowrate (*sccm*)	SiH_4	20	20	20	2.8
	PH_3	—	1	—	—
	B_2H_6	—	—	3.5	—
	H_2	—	—	—	100
	NH_3	—	—	—	150
Pressure (*mTorr*)		375	400	480	500
Substrate temperature (°*C*)		150	150	150	250
Time (*min*)		30	30	30	45
RF power (*Watt*)		1	1	1	1
Desired thickness (*nm*)		200	200	200	300
Measured thickness (*nm*)		—	230	—	340

A SiN_x layer was deposited on top of an amorphous silicon layer by PECVD. The parameters for these two continuous depositions are listed in Table 3-3. Mask 2 was used to align and pattern the silicon gates. In the table, the measured thickness is obtained from Tencor® Profilometer during the fabrication.

The silicon material deposited by PECVD in this work is initially amorphous. After diffusion and drive-in process, the amorphous silicon will be doped and crystallized, this can lead to a higher conductivity for the silicon gates.

Intrinsic, p^+ and n^+ amorphous silicon were deposited and studied. Although it has been known to cause potassium contamination in MOSFETs, we used KOH in the c-Si MOSFET fabrication process because it was an in-house etching solution that we had previously developed for our PECVD a-Si film. KOH has been used in the past[24] as a wet etchant for a-Si films in transistor fabrication. The reaction for the silicon etching is as following at 35°C:



$$Si + H_2O + KOH \rightarrow K_2SiO_3 + H_2 \uparrow \qquad (3\text{-}5)$$

The crucial problem for silicon pattern is the uneven etching result. The first several silicon etching tests in this study all got uneven results and some silicon gates are even missing. The possible reason is the hydrogen generated in the process. During the etching, the KOH will etch the very surface of the silicon film, which could generate hydrogen in the form of bubbles. These hydrogen bubbles accumulate in the film surface and insulate the KOH from silicon.

There are two methods to solve this problem. The first is adding IPA (Iso-propyl alcohol). The purpose of IPA is to make the etching more uniform by removing the bubbles near the film surface. The etchant for silicon etching in this study follows the mixture below:

800 ml DI water

240 g KOH

230 ml propanol

The second method to improve etching is agitation. Agitating the silicon wafer or the solution during etching will promote the final etching result significantly by removing the hydrogen soon after its generation.

For 230nm silicon film, it took about 7~8 minutes to complete the etching. The Si gates and test structures were patterned clearly. Etch rate for amorphous Si (intrinsic and n^+) was measured to be 30 nm/min.

Intrinsic and n^+ amorphous Si are successfully patterned by KOH solution; while, this is not applicable for p^+ a-Si. Boron is introduced into Si during the PECVD deposition to produce p^+-type film. Literature [25] shows that high levels of boron in silicon will reduce the rate at which it is etched in KOH by several orders of magnitude, effectively stopping the etching of the boron rich silicon. For this reason, p^+ a-Si was not chosen as the gate material for MOSFET in this study.

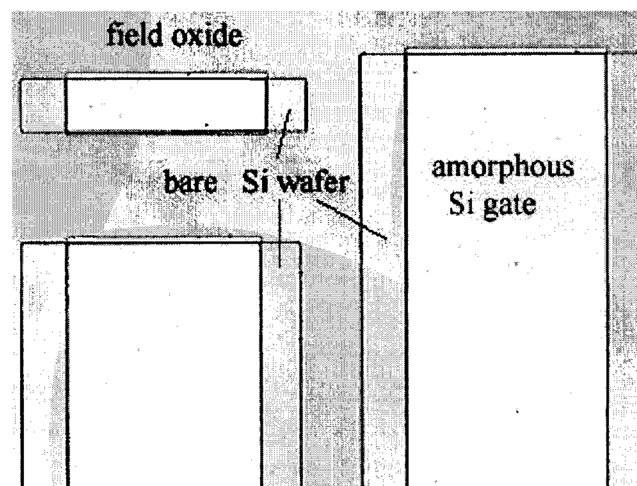


Figure 3-15 Structures after open D/S windows.

After Si has been patterned, drain/source windows should be opened for the next step — diffusion. Buffered HF solution was used to etch the oxide and SiN_x. Figure 3-15 shows the structures after D/S windows have been opened. The etch rate for SiN_x is much faster than oxide and Si gates will be exposed after the windows are completely opened. Thickness measurement by Tencor® Profilometer was used to determine the end point of etching during Si pattern and D/S windows opening. By measuring the thickness profile, Figure 3-16 shows the structure of MOSFET after D/S windows opening.

The 340nm SiN_x can be removed completely in about 80 seconds. The etch rate for low power PECVD SiN_x is 250 nm/min.

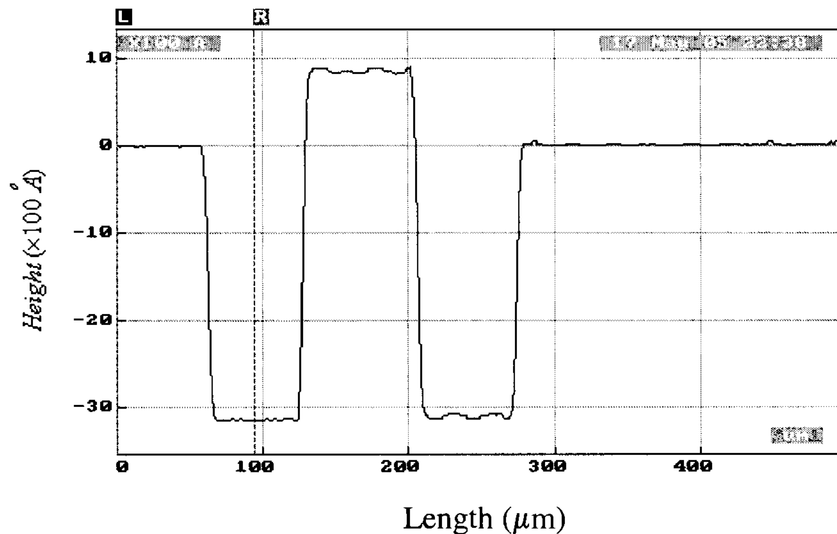


Figure 3-16 Profile of MOSFET after D/S windows opening.

3.3.2.4 Boron/phosphorous diffusion and drive-in

After Si pattern and D/S window opening, the wafer was ready for diffusion process.

Boron diffusion was done on n-type wafer for p-channel MOSFET (diffusion source BN975, made by Saint-Gobain Advanced Ceramics Corp.). The wafer had been

cleaned by standard RCA before went into the diffusion furnace. Because p^+-doped a-Si can not be patterned by KOH etchant used in this study, intrinsic a-Si was employed as the gate for the p-channel MOSFET.

Phosphorous diffusion was performed on p-type wafer for n-channel MOSFET (diffusion source PH1000N, made by Saint-Gobain Advanced Ceramics Corp.). We chose n^+ a-Si as the gate material for its higher conductivity, although intrinsic and n^+ a-Si both can be used for n-channel MOSFET.

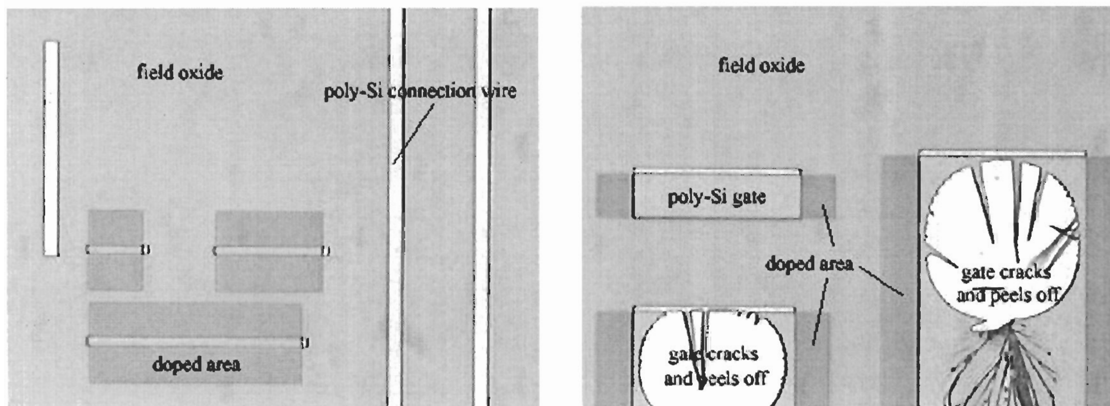
A drive-in process was performed immediately after the diffusion had been done. The purpose of drive-in is to act as "limited-source diffusion", which can increase the diffusion depth of the previous "infinite-source diffusion".

Table 3-4 shows the parameters for the steps. The diffusion and drive-in steps are both performed under high temperature, which also can anneal the a-Si at the same time. The annealing was done well on the small area of Si; while, for an area of $80 \times 80 \mu m^2$ or larger, the Si film cracked after the high temperature annealing because of thermal stress.

The different thermal coefficient between Si and oxide might be the reason for the cracks. When temperature was ramped up and down, the film will expand and shrink correspondingly. With different thermal coefficient, the Si and oxide will not expand and shrink simultaneously, which leads to a stress in between. The stress is dependent on the thickness and area of the film. When the film area is large enough, the stress will increase beyond the tolerance of the film and cracks occur. Figure 3-17 shows the Si after phosphorous diffusion and drive-in. We can see from the graphs that small area Si is in good shape while large area Si cracks.

Table 3-4 Parameters and functions of diffusion and drive-in process.

	Boron (p^+)	Phosphorous (n^+)	Drive-in
Temperature (°*C*)	1000	1000	1000
Time (*min*)	40	40	30
N_2 flowrate (*scfh*)	4	4	4
Step function	1. Deposit a layer of glass containing the impurity wanted on the surface of the doping area; 2. Anneal the a-Si.		1. Increase the diffusion depth by driving the impurity into the doped area; 2. Anneal the a-Si.



(a) gate and connection wire in APS array (b) large area Si gate cracks and peels off

Figure 3-17 Structures after phosphorous diffusion and drive-in.

3.3.3 Passivation layer, contact via holes and aluminum patterning

After boron/phosphorous diffusion and drive-in, an additional layer of SiN_x was needed on top of the wafer to serve as passivation layer. Contact via holes will be opened on this SiN_x layer using Mask 3.

The SiN_x layer was deposited by PECVD using the same parameter mentioned in Table 3-3. The etchant for pattern SiN_x is Buffered HF. 90 seconds was used to open the contact via holes completely and a little of overetch.

With its high electrical conductivity, Al is a popular material for electrodes and wire connections in semiconductor devices and circuits. Al was used as the electrodes for the devices and circuits in this study. 1μm-thick Al was deposited by sputtering as the electrodes and interconnects for the devices.

Mask 4 was used for Al patterning, which was the final step during the fabrication process. Bottled aluminum etchant was used for the etching and the etch rate is 100Å/sec at 50°C as stated on the bottle of the etchant. The components for aluminum etchant are phosphoric acid, acetic acid and nitric acid and are similar to the PAN etchant for Mo etching. For 1μm-thick Al 100 seconds were used for completely pattern. Figure 3-18 shows the structures after Al patterning was done.

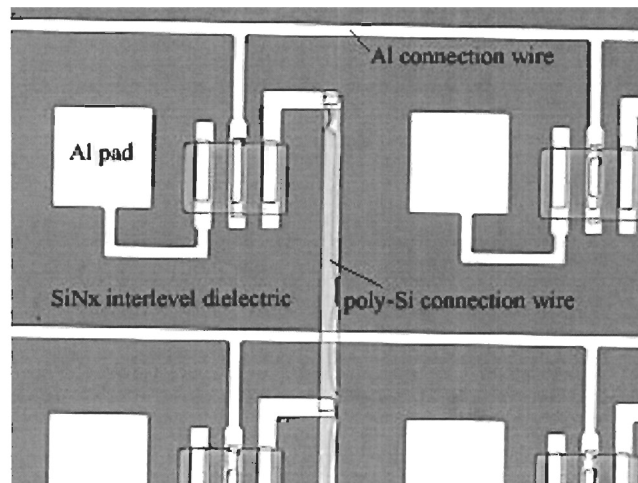


Figure 3-18 Structures after Al patterning.

The fabrication process was complete after Al patterning. To get a better contact between the Al electrode and Gate/Source/Drain, the fabricated device was annealed for another 3 hours in air at the temperature of 150°C.

3.3.4 Discussion on fabrication process for self-aligned MOSFET

After the operation of whole fabrication, some problems about the mask and fabrication were discovered and expected to be improved during the subsequent research.

Si etching

Constant agitation is the key issue for uniform Si etching. Iso-propanol and frequently manual stirring were used as agitation in this work. For better pattern results, mechanical agitation source is desired to replace manual stirring.

Overlaps between structures

The tolerance for fabrication process depends on the possible alignment errors, feature size, etc. Overlap between different structures indicates the process tolerance for alignment errors. Enough space for overlap should be included in design to ensure fabrication validity. If there is no enough overlaps between structures, when misalignment happens and the structures shift from the supposed position, the devices would lose its original properties. In this work, limited overlaps were designed between part of MOSFET gates and contact via holes. The gate and via holes will shift to each other when misalignment occurs. Figure 3-19 shows this error on an n-channel MOSFET.

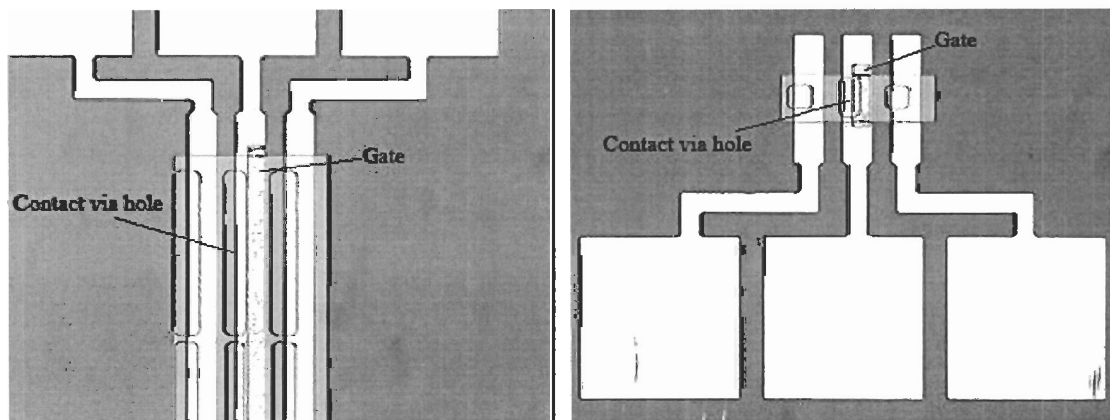


Figure 3-19 Insufficient overlaps between gate and contact via hole.

CHAPTER 4 DEVICE ANALYSIS

After the design and fabrication process, n-channel MOSFET devices on p-type wafer and p-channel MOSFET devices on n-type wafer were fabricated. In this chapter, properties of the devices and test structures on the silicon wafers were measured and discussed.

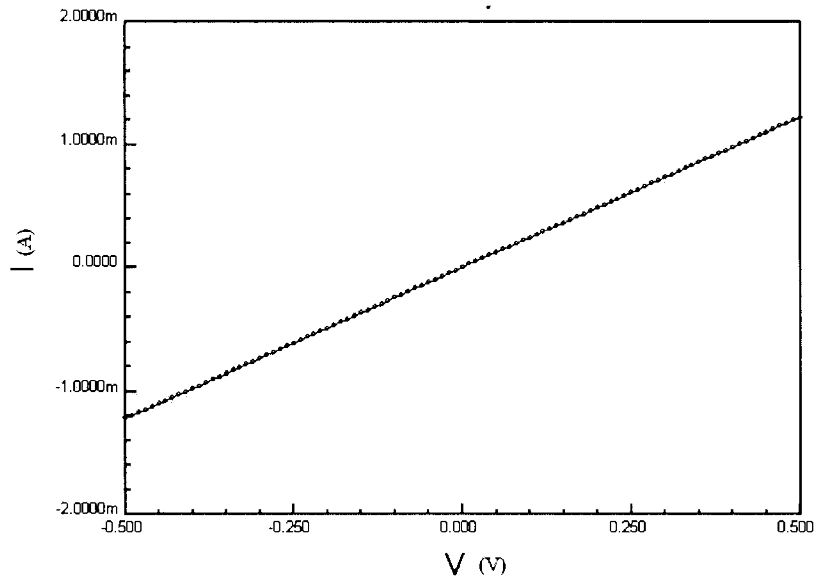
For convenience, we name the n-channel MOSFET devices on p-type wafer as "nMOS sample", and the counterpart, "pMOS sample".

4.1 Continuity/isolation test

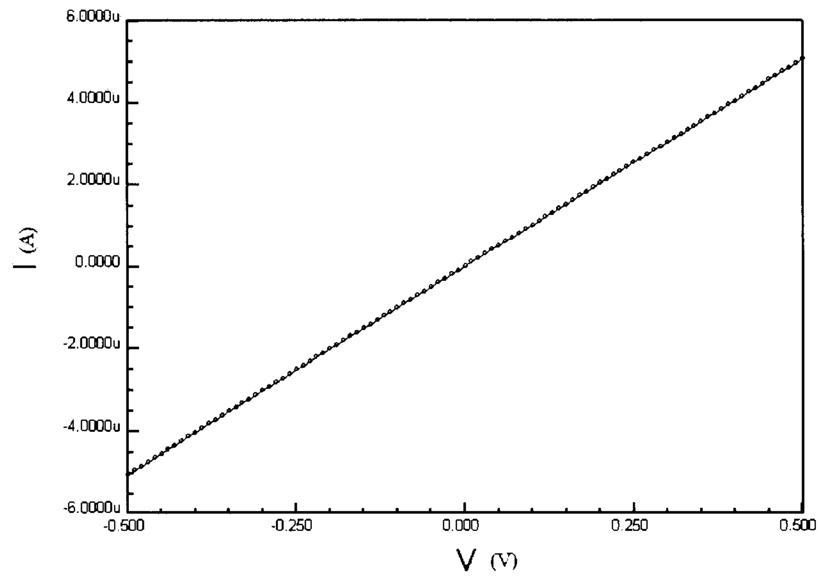
During the fabrication process, an imperfect etch, like overetch or incomplete etch, is possible. This imperfection can lead to unwanted broken wires or the connection of wires among different devices. To check the integrity of the connection wire during fabrication process, continuity/isolation tests were performed prior to the testing of material and device properties. The structures used in this test are shown in Figure 3-14.

I-V measurements were performed for both Si and Al wires. For non-error fabrication, the result of the continuity test should be a straight line exhibiting the property of a resistor. The Figure 4-1 shows the I-V curve for the continuity structures with different material.

For the isolation test, the two pads need to be open under correct operation, due to which a high resistance is obtained, and the I-V curve for the test superimposes with the X-axis. Figure 4-2 depicts the I-V curve for the isolation structures on Al structure.



(a) Continuity test on Al structure



(b) Continuity test on Si structure

Figure 4-1 Continuity test on Al and Si test structures.

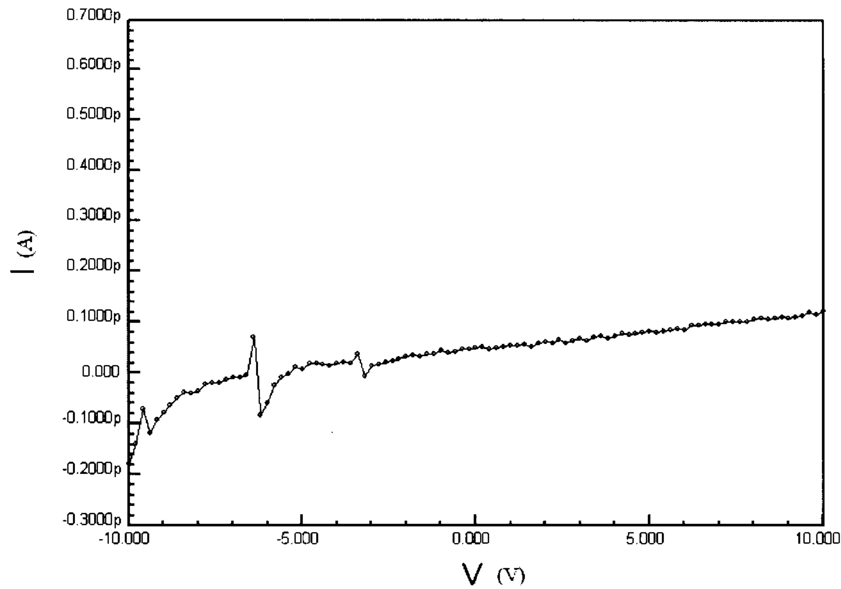


Figure 4-2 Isolation test on Al test structure.

4.2 Capacitance-voltage measurement on MOS capacitor structures

4.2.1 Interface state density

The energy-band diagram of a semiconductor at the oxide-semiconductor interface is shown in Figure 4-3 [26]. The periodic property of the semiconductor is abruptly terminated at the interface so as to allow the existence of electronic energy levels exists within the forbidden bandgap. These allowed energy states are referred to as interface states.

Charge density of the inversion layer in MOS structure can be changed by two types of mechanisms: diffused minority carriers across the space charge region from the substrate and thermal generation of electron-hole pairs within the space charge region. Both these processes generate charges at a particular rate. The charge concentration at the inversion layer can not change simultaneously. At low frequency bias, the charges have sufficient time to respond and saturate. If the voltage frequency across the MOS capacitor

is too high, the minority carrier response in inversion does not saturate, and thus the capacitance in this bias region will not evaluate to the saturated value [27]. When the frequency is high enough, the minority carriers do not respond. This property leads to the difference of C-V curves low and high frequency. In general, the range for low frequency of MOS capacitor is from 5 to 100 Hz, and the value for high frequency is 1 MHz.

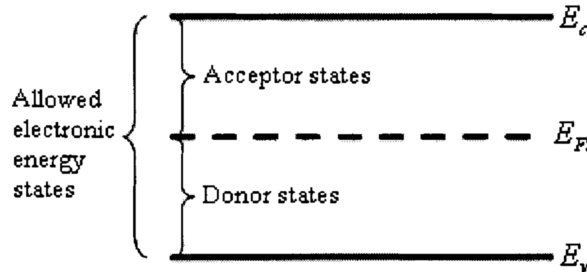


Figure 4-3 Interface states of oxide-semiconductor interface.

Oxide-semiconductor interface state density can be determined through HLCV (high-frequency and low-frequency C-V) measurement. This combined high-low frequency capacitance method was first proposed by Castagnè and Vapaille [28], and can eliminate the device's need for measurement of its doping profile. Figure 4-4 shows the measured QSCV (Quasi-static CV) curve.

Interface state density can be calculated from the formula (4-1) [28].

$$D_{it} = \frac{C_{ox}}{A \cdot q}\left(\frac{C_{ox} - C_{LF}}{C_{LF} \cdot C_{ox}} - \frac{C_{ox} - C_{HF}}{C_{HF} \cdot C_{ox}}\right) \qquad (4\text{-}1)$$

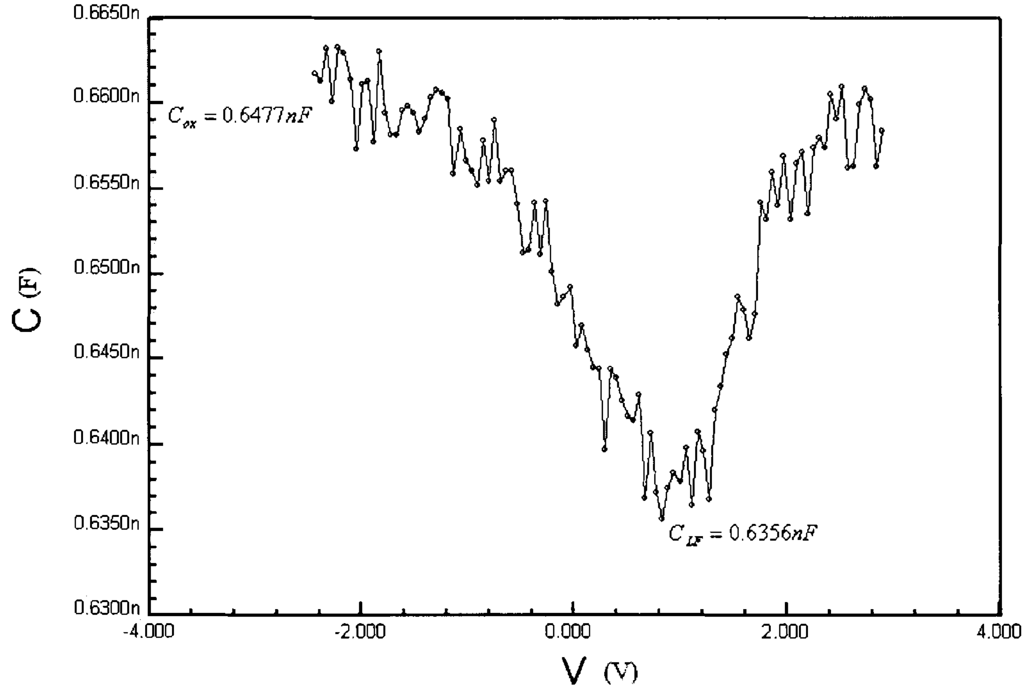


Figure 4-4 QSCV curve for MOS capacitor on p-type wafer.

In the formula, A is the area of MOS capacitor, D_{it} is interface state density, C_{ox} is the capacitor of MOS structure, C_{LF} is the lowest point on the LF C-V curve, and C_{HF} is the point on the HF C-V curve that corresponds to the voltage where C_{LF} occurs.

HLCV measurement can be realized through simultaneous or sequential-measuring method [28]. Simultaneous-measuring method is to measure the C-V relation under high frequency and low frequency at the same time. Sequential-measuring method, on the contrary, will measure the high frequency and low frequency C-V curves step by step. In this work, sequential-measuring method was used by using the available equipment.

In our measurement, $C_{ox} = 0.6477nF$, $C_{LF} = 0.6356nF$ and the corresponding $C_{HF} = 0.2897nF$. The designed capacitor area $A = (0.18 \times 0.18)cm^2$ and electronic

charge $q = 1.60\times10^{-19}C$. Interface state density can be calculated from Formula (4-1) that gives $D_{it} = 6.4539\times10^{12}[eV\cdot cm^2]^{-1}$.

By comparison we can see that the interface state density for the sample is one or two orders of magnitude higher than the value recorded in existing literature [29, 30] that are in the range of $10^{10} \sim 10^{11}[eV\cdot cm^2]^{-1}$. The contaminated furnace tube is the primary reason for the higher interface state density. The curve was affected by noise too. A high state density in oxide-semiconductor interface indicates the presence of high intrinsic defects in the near-interfacial oxide layer [31, 32]. These defects will degrade the carrier mobility in the channel, thus negatively influencing the speed of MOS devices. High interface state density can also create states in the fundamental band gap effectively reducing the band gap of the insulator. These states can be occupied under thermal excitations, and hence cause conduction [33]. Combination of interface states and charges in oxide are the main elements that lead to the leakage current in the MOS devices. The high interface state density between oxide-Si in this work may cause inferiority for the device fabricated. Influences of interface states and oxide charges will be discussed in the next section.

4.2.2 Capacitance-voltage measurement and analysis

C-V measurements are a valuable diagnostic tool to characterize a MOS device. In this work, C-V measurements were performed to check the property of oxide used for the gate dielectric in the MOSFET.

A C-V measurement was initially done on the pMOS sample (n-type wafer). Figure 4-5 compares the sample C-V plot with the more perfect C-V curve obtained from

previously grown oxide. The oxide thickness and capacitor area of the two MOS capacitors for the measurements were the same to provide a comparable result.

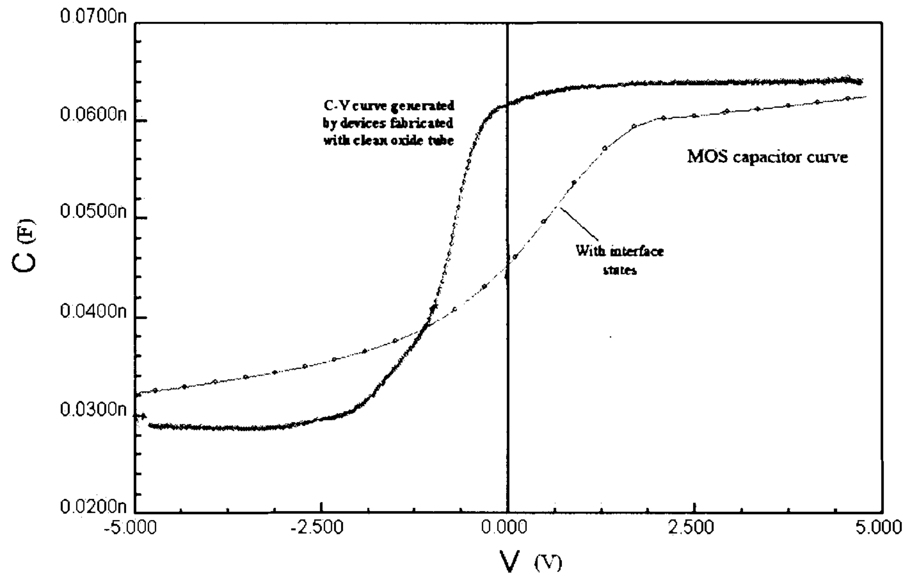


Figure 4-5 Comparison of C-V curves for pMOS sample (n-type wafer) and "ideal" curve.

We can see that the C-V curve on pMOS sample is influenced by noise, gets leveled and shifts from the original place.

The oxide used in the MOS structure was grown right after a thorough clean of the thermal oxide growth tube. The process of dopant drive-in also performed in the same thermal oxide tube, which may lead to degradation of oxide growth, on possible contaminants in the tube.

The non-ideal effects in MOS capacitors could be the reason for the leveled curve and curve shift. Non-ideal effects in MOS capacitors include fixed charge, mobile charge and surface states charge. When interface states are present, the amount and direction of the shift changes as we sweep through the gate voltage; this change is due to the change in the amount and sign of the interface trapped charge [26]. Interface states lead to the

leveling of the C-V curve. The interface states cause the transition in the capacitance measurement to be less abrupt, as shown in Figure 4-5. As stated in previous section, the amount of curve level-up can be used to determine the density of interface states through the combination of low and high frequency measurements of the capacitance.

The positive fixed oxide charges result in the negative-direction shift of the C-V curve. The fixed oxide charges are likely caused by ions introduced during the growth. Therefore, device fabrication should be kept at a certain level of impurities. A positive fixed charge at the oxide-semiconductor interface shifts the flat-band voltage by an amount that equals to the ratio of the charge and oxide capacitance.

Different from the one-direction C-V shift caused by fixed oxide charge, the C-V shift caused by mobile charge changes direction according to the positive/negative gate voltage. A positive gate voltage attracts negative mobile charge towards the gate electrode, while a negative voltage repels the charge away from the gate. This movement causes the curve to shift towards the applied voltage. The hysteresis on C-V curve occurs due to the back-and-forth sweeping of the gate voltage. The mobile charge is likely due to the sodium or potassium ions incorporated in the oxide during the fabrication. The industry carefully controls the purity of the water and the chemicals used [34], which is because of the high sensitivity of MOS structures to a variety of impurities. Ion-drift type hysteresis may have occurred on device C-V characterization [35~37] because of the KOH etchant we used during fabrication. Figure 4-6 shows the C-V hysteresis in this study. The C-V curve was measured on the MOS capacitor fabricated and tested, details of which have been discussed in Chapter 2.

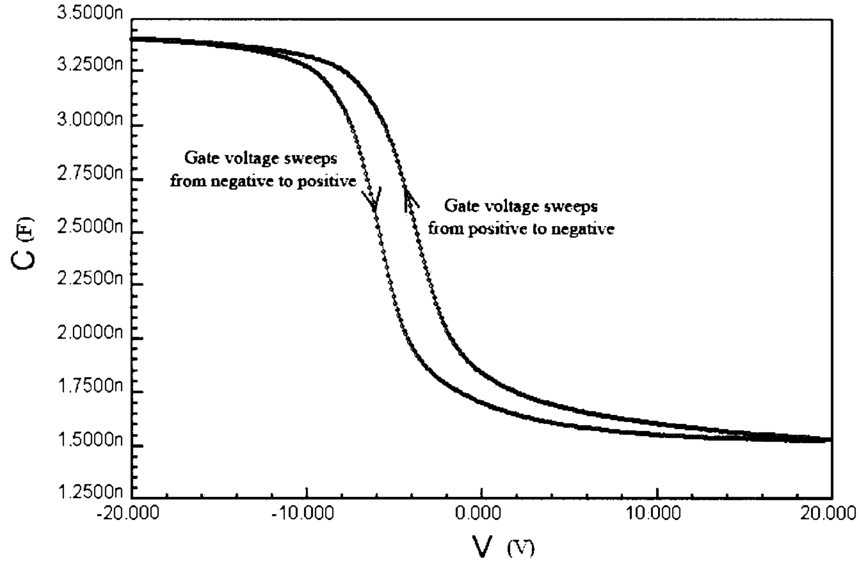


Figure 4-6 Mobile charge induced C-V curve hysteresis on p-type wafer.

The C-V curve on nMOS device (p-type wafer) is shown in the Figure 4-7. The curve is still affected by noise and exhibits a leveling effect. Gate oxide with inferior property might cast a negative influence on the MOS devices. Some of these influences could be device leakage current, threshold voltage (V_T), and Current-Voltage (I-V) curve.

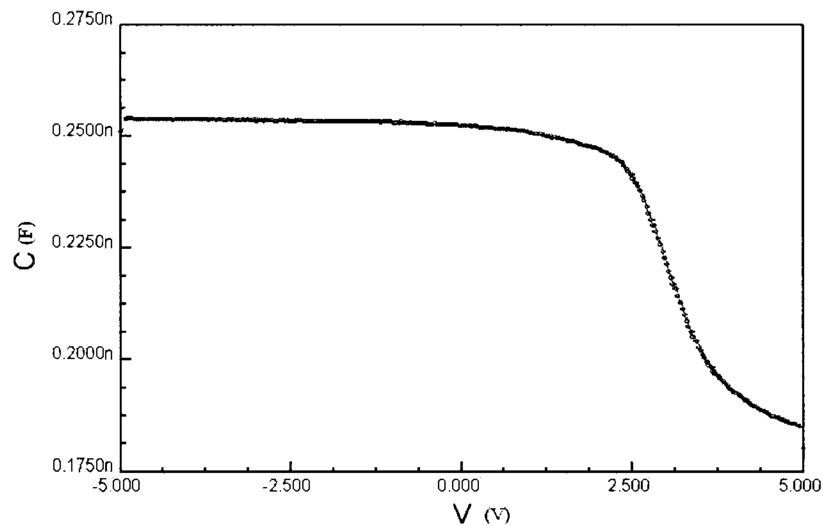


Figure 4-7 C-V curve on nMOS sample (p-type wafer).

4.3 TLM test structure

TLM test structure can be used to test the contact resistance R_c and sheet resistance R_s. Figure 4-8 shows the lateral current flow of the TLM structure.

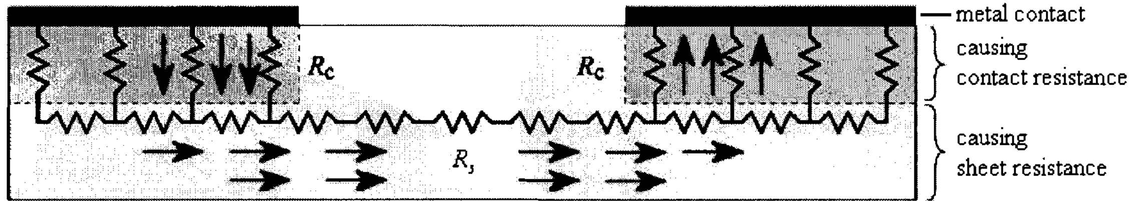


Figure 4-8 Lateral view of current flow in TLM structure.

From the figure, we can see that the total resistance R_T between two metal contacts can be expressed by the formula below.

$$R_T = R_s + 2R_c \tag{4-2}$$

Contact resistance exists between the test probe and aluminum pad and between the aluminum pad and silicon. We will ignore the contact resistance between the probe and the pad, and concentrate on the resistance between the pad and the silicon. Contact resistance is determined by

- Size and shape of the contact
- Silicon type and doping concentration
- Annealing condition
- Direction of the current flow [38]

The basic TLM structure used in this work is shown in Figure 4-9. The test dimensions are listed in Table 4-1.

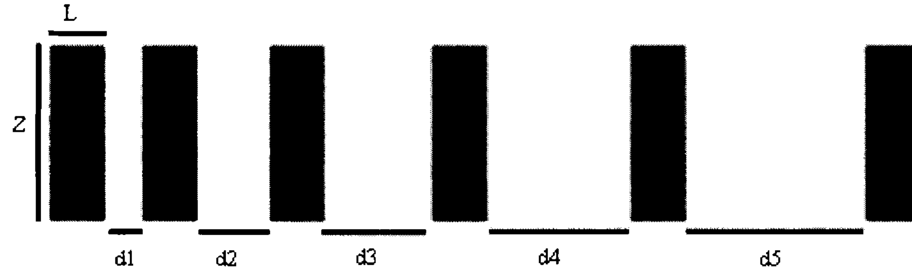


Figure 4-9 TLM structure in this work.

Table 4-1 Dimensions of TLM test (unit: μm).

Z	L	d				
		d_1	d_2	d_3	d_4	d_5
190	200	30	35	40	45	50

During I-V measurement, two probes were used to touch the neighboring contacts and apply a sweeping voltage. Agilent® 4156C Semiconductor Parameter Analyzer was employed to test the current, as the voltage sweeps. The I-V curve for each measurement is a straight line with a slope that characterizes the resistance between the two contacts. Four corresponding total resistances were obtained, which can be plotted as a function of contact distances, as shown in Figure 4-10.

As labeled in Figure 3-11, after calculation, we can get the resistances:

$$R_c = 17.72\Omega\,,\ \ R_s = 57\Omega / \square$$

The n^+ Si film was doped during PECVD deposition and thermal diffusion. In thermal diffusion and annealing process, the Si film could also be partly crystallized. These processes can reduce the sheet resistance of the Si film. This sheet resistance is acceptable by comparison with [39], which has similar deposition and annealing

conditions as used in this work. The low sheet resistance and contact resistance provide a low R ohmic contact for the MOS devices.

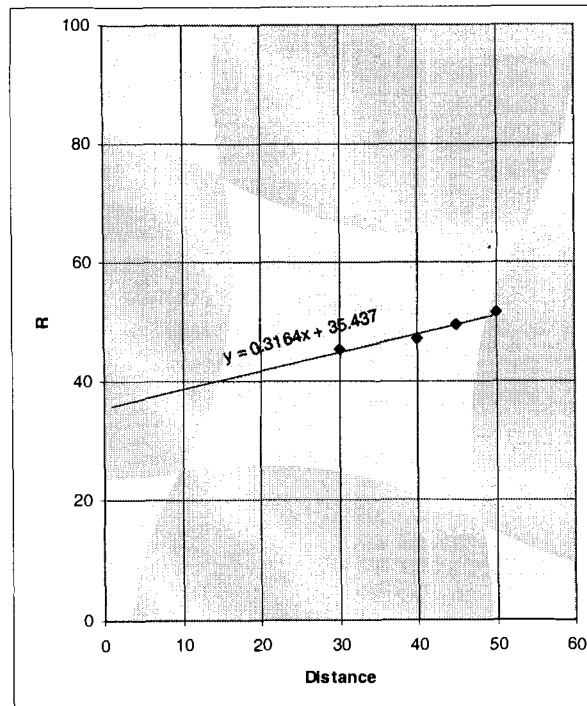


Figure 4-10 Plot of total resistance as a function of contact distance.

4.4 Current-voltage characteristics of MOSFET

The current in MOSFET is due to the charge flow in the inversion layer (channel) adjacent to the oxide-semiconductor interface. The MOS devices can be classified into two categories depending on the charges in the channel: enhancement-mode and depletion-mode. Inversion layer will not be created unless gate voltage is applied in enhancement-mode devices. For depletion-mode MOS devices, the conducting channel between drain and source already exists at zero gate voltage. High interface state density could be the reason for the presence of conducting channel at zero gate voltage.

Appendix 1 describes the operation theory and current-voltage characteristics of MOSFET. Current-voltage (I-V) measurement on MOSFET helps to characterize the MOS devices fabricated in this work.

I-V measurement on a packaged MOS device (made by ON® Semiconductor) was performed to get a standard plot. The measurement was realized by Agilent® 4156C Semiconductor Parameter Analyzer and SIGNATONE® probe station, which are controlled by computer through the connection of GPIB. Figure 4-11 is the plot for drain current versus drain voltage of the packaged nMOSFET under gate voltage $V_G = 1.5V$.

From the plot, we can see that the nMOS is initially in linear region. Once the drain voltage reaches $V_D = 1.8V$, nMOS goes into saturation region. The $I_D - V_D$ plot reveals favorable characteristics of the packaged MOSFET.

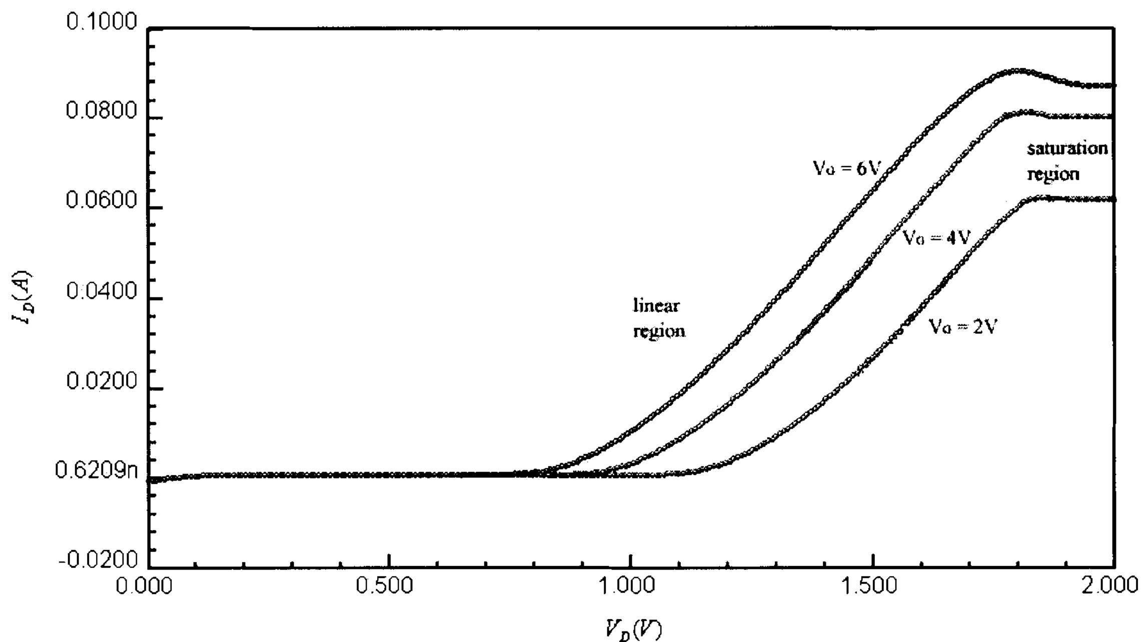


Figure 4-11 Drain current as a function of drain voltage for packaged nMOSFET.

4.4.1 NMOSFET and PMOSFET characteristics

N-channel MOSFETs were fabricated on p-type Si wafer. Drain current I_D versus gate voltage V_G were measured, keeping the drain voltage V_D constant. Figure 4-12 shows $I_D \sim V_G$ curve for nMOSFET and pMOSFET, when $V_D = 0.5V$, V_g sweeps from $-3V \sim 0V$.

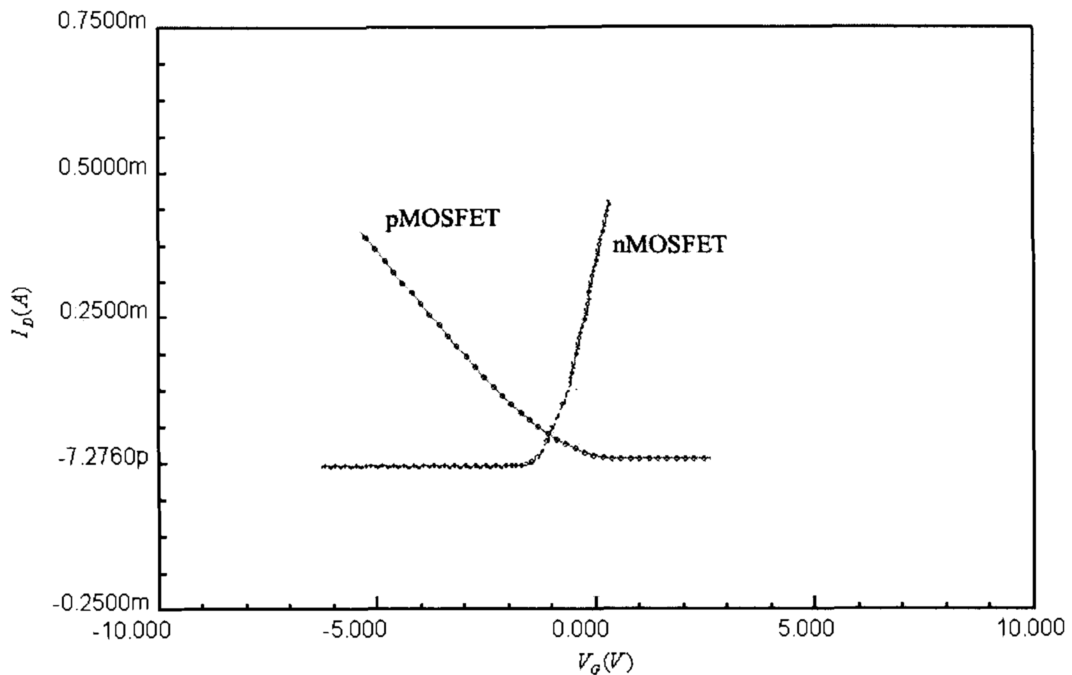


Figure 4-12 I_D as a function of V_G for nMOSFET and pMOSFET (V_D=0.5V).

In the plot, when $V_G = 0$, if a V_D is applied on the drain contact, a small I_D continue to exist. This phenomenon indicates that the nMOS device is in depletion mode. This mode may have originated from the high interface states between the oxide and semiconductor. The interface state density used for nMOS devices is around $6\times10^{12} \sim 8\times10^{12}[cm^2 \cdot V]^{-1}$, which is one or two orders of magnitude higher than the requirement of the enhancement-mode device. A very high interface state density will

lead to extra carriers in the oxide-semiconductor interface, thus conducting a channel without the application of gate voltage. If there is a voltage between drain and source, corresponding current will be generated.

Leakage current also exists during the operation of MOSFET. In theory, there should be no inversion layer charge below the threshold voltage. Zero current is expected below the threshold voltage. But the actual subthreshold-voltage current is not zero and can be expressed in the following formula:

$$I_D \propto \exp(\frac{V_G - V_T}{V_t}) \qquad (4\text{-}3)$$

In the formula, V_T is the threshold voltage of MOSFET, and $V_t = 0.0259V$ is the thermal voltage.

Leakage current measured in this work is in the range of $pA \sim nA$, with a typical value of $10pA$.

Oxide charges inside the dielectric film can act as electron traps and hence create conduction pathways, while a high interface state density creates states in the fundamental band gap effectively reducing the band gap of the insulator. These states can be occupied under thermal excitations and hence can cause conduction. Other reasons accounting for leakage current include junction leakage, gate oxide tunneling, and hot-carrier injection.

I_D versus V_D curves for NMOSFET and PMOSFET are shown in Figure 4-13. In the plot, curves for nMOSFET are in the linear region. If V_D increases beyond $3V$, I_D will increase accordingly and the curve maintains a linear shape until it reaches the upper

current range of the Agilent® 4156C. This phenomenon indicates that the MOSFET can not be saturated with the ramping up of drain voltage. The pMOS devices are in enhancement mode and contain a conducting channel when no gate voltage is applied. Leakage current for pMOS is in the range of pA and the typical value is $20pA$. From the curves for pMOSFET, we can see that the curves could reach saturation but influenced by saturation modulation effect.

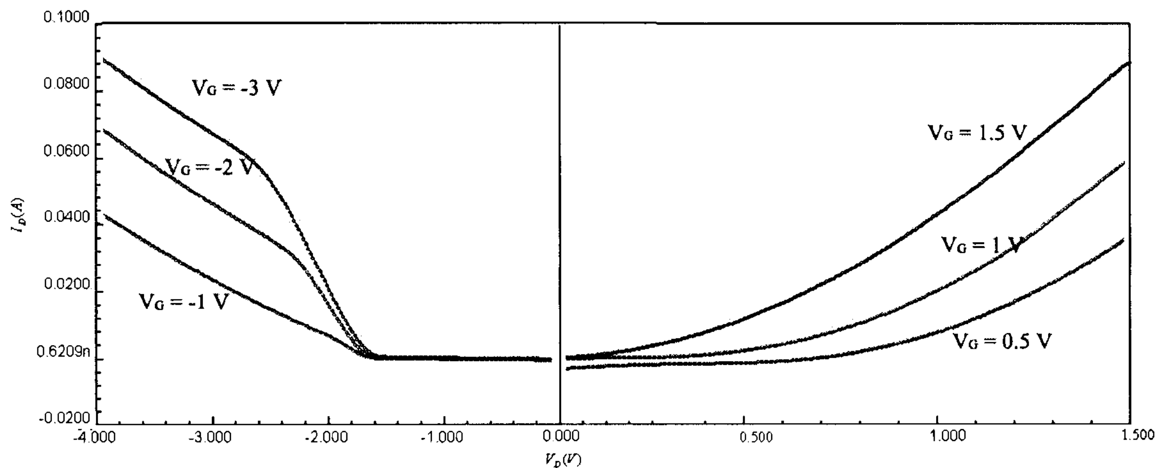


Figure 4-13 I_D as a function of V_D for nMOSFET and pMOSFET.

Non-saturation phenomenon can occur when the resistance between G/S and G/D are very large [40]. Self-aligned MOSFET can avoid the error by the unique self-aligned structure. The reason for the non-saturation MOSFET might result from misalignment during fabrication. The unwanted shift of contact via holes, originating from misalignment in fabrication, could also cause problem for the MOS devices. When misalignment happens for the third mask step, large contact via hole shift may not only expose the supposed gate area, but also part of the drain or source area. This error is carried forward to the next step. After the patterning of top contacts, the aluminum

contacts for gate touch the gate as well as the drain or source doped area. Figure 4-14 explains the error by showing a section view of the structure.

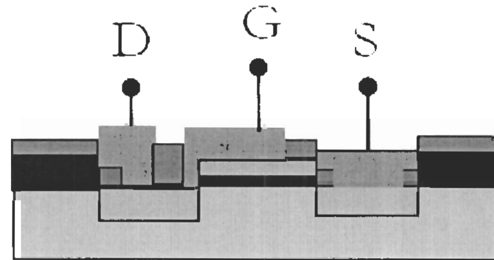


Figure 4-14 Contact via hole shift because of misalignment.

When contact via hole shift happens the gate electrode can contact gate and drain/source doped area at the same time.

$V_G = V_S = 0$ when gate and source are shorted in MOSFET. Thus there is no gate voltage applied on the MOSFET. For the depletion-mode MOSFET, a conducting channel already exists when gate voltage is zero. Once the drain voltage is applied, I_D can be created in the channel. A non-saturation region in the $I_D \sim V_D$ curve can be observed in the measurement. Measurements on this unwanted shift have been done, both for gate-drain short and gate-source short.

For shorted gate and drian, $V_G = V_D$. As the nMOSFET is in depletion mode, and $V_T < 0$, there always exist

$$V_D < V_G - V_T \tag{4-4}$$

In this case, MOSFET is always in linear region and cannot reach saturation.

4.5 Uniformity of devices

4.5.1 Threshold voltage measurement

The uniformity of the devices fabricated in this work can be checked by comparing the measurement results.

Due to uneven Si etching for pMOS sample, part of the gates were destroyed, which leads to characterization of only devices on the dies around the wafer edge. The device uniformity on wafer was mainly performed on nMOS sample.

As shown in Figure 4-15, the dies on the wafer were numbered from 1 to 8.

The threshold voltages of the nMOS sample on each die were measured and are listed in Table 4-2. Because of errors during the fabrication, gates in the center dies (die 1 to die 4) on pMOS sample were missing. The available threshold voltages on pMOS sample were measured and listed in Table 4-3.

The errors are predictable and are due to the fabrication because of imperfect alignment and layer pattern. To minimize the fabrication errors using the available facilities, promotion of mask design, mastery of the properties and processes in every steps, great patience and carefulness are the crucial elements.

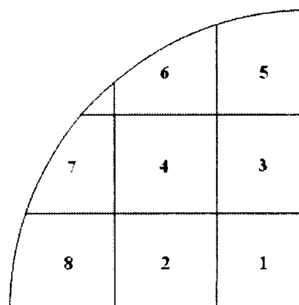


Figure 4-15 Numbers of dies on wafer.

Table 4-2 Threshold voltage on depletion-mode nMOS sample.

Die	Threshold voltage V_T (V)
1	-1.21
2	-1.23
3	-1.22
4	-1.27
5	-1.29
6	-1.41
7	-1.40
8	-1.30

Table 4-3 Threshold voltage on pMOS sample.

Die	Threshold voltage V_T (V)
5	-0.98
6	-0.93
7	-1.03
8	-0.90

4.5.2 Interface state density calculated by threshold voltage

The formula for threshold voltage is [26]

$$V_T = (Q'_{SD} - Q'_{SS})\frac{t_{ox}}{\varepsilon_{ox}} + \Phi_{ms} + 2\Phi_{fp} \tag{4-5}$$

where V_T is threshold voltage, Q'_{SD} is surface charge density per unit area of depletion region, Q'_{ss} is oxide interface charge density, t_{ox} is gate oxide thickness, ε_{ox} is oxide permittivity, Φ_{ms} is work function between metal and semiconductor, Φ_{fp} is the difference between E_{Fi} and E_F.

Surface state density can be calculated from the formula (4-6)

$$D_{it} = \frac{Q'_{ss}}{e} \qquad (4\text{-}6)$$

where electronic charge $e = 1.60 \times 10^{-19} C$.

Take die 7 of pMOS sample for example, where threshold voltage $V_T = -1.03V$, doping level of p-type silicon wafer $N_a = 3 \times 10^{17} cm^{-3}$, oxide thickness $t_{ox} = 200nm$. Oxide interface charge density can be calculated from Formula (4-5), where $Q'_{ss} = 3.04 \times 10^{-7} C / cm^2$. Thus, interface state density can be obtained from Formula (4-6), where $D_{it} = 1.90 \times 10^{12} [eV \cdot cm^2]^{-1}$. Compare this value with the value we obtained from HLCV measurement, which is $D_{it} = 6.4539 \times 10^{12} [eV \cdot cm^2]^{-1}$, we can get the conclusion that the characterizations of MOSFETs in this chapter reflected the device properties properly.

CHAPTER 5 SUMMARY

5.1 Overview

The general goal of this work was to design and develop an in-house fabrication process for self-aligned MOSFET on silicon substrates at SFU.

The entire process includes dielectric material growth and test, photo mask design, device fabrication, and characterization. Two materials were grown and tested. Silicon dioxide, as gate dielectric, was grown by thermal oxidation on silicon substrate. Silicon nitride was deposited by PECVD to serve as interlevel dielectric. C-V and breakdown measurements are employed to check the availability of the two dielectrics. Mask set was designed by Cadence®. Entire fabrication steps were performed at SFU IMMR fabrication facility. After the completion of fabrication, characterizations on the devices and test structures were carried out to check the material and device properties.

5.2 Summary of contributions

The oxide was grown thermally under 1100°C, by both wet oxidation and dry oxidation, which are for field oxide and gate oxide, respectively. The function of field oxide is to insulate different devices on the wafer.

C-V and breakdown measurements were done to check the availability of gate oxide and SiN_x. Computer console was controlled by the ICS software.

From the C-V measurement, the oxide and SiN_x show smooth curves, except for a little bump in the oxide C-V curve. This bump results from the abnormality of the surface

states in the oxide. Impurity introduced during the thermal growth may lead to the high surface states in the oxide. After the thermal tube was cleaned thoroughly, the oxide was grown again. This oxide showed acceptable C-V curves. During the breakdown measurements, both oxide and SiN_x show favorable characteristics and are sufficient to be gate dielectric and interlevel dielectric.

Mask set was completed using Cadence® design kit. Based on the structure of self-aligned MOSFET, a total of four mask-layers were required. A 4-in-1 mask set was proposed and implemented during the design.

The fabrication process was carried out in the 100 class level cleanroom. Molybdenum as the gate material was initially selected for its high melting temperature and excellent electrical conductivity. When temperature exceeds 500°C, Mo may react with oxygen. In addition, the internal stress may also cause the Mo film to peel off. Alternatively, poly-Si gates were developed by starting with amorphous, doping during deposition and thermal annealing during diffusion can alter the a-Si to poly-Si.

Wet etch was used to open the windows necessary for devices. Etch rates for wet oxide, dry oxide, SiN_x, a-Si and Al were tested and recorded. Accurate controls of etch time and fabrication parameters (temperature, solution agitation, etc.) are crucial for the fabrication. A-Si patterning was one of the most challenging steps in the fabrication. KOH solution was selected as the basic a-Si etchant. Si gate has been patterned successfully.

Another fact about silicon gate that should be noticed is the patterning for boron-rich (p^+) amorphous silicon. Experiments showed that the etch rate for boron-riched

amorphous silicon is several orders of magnitude lower than the etch rate for phosphorous-riched (n^+) or intrinsic amorphous silicon.

Self-aligned MOSFET and test structures were fabricated successfully after a series of steps. C-V and I-V measurements were performed to test the device properties. C-V measurements indicated that the oxide property was not as good as the sample grown right after the tube clean and could cause device degradation. The n-type MOSFET devices have a conducting channel when no gate voltage is applied, which indicates they are in depletion mode. The devices can not reach saturation region with increasing drain voltage. Short between drain and gate area originated from misalignment may account for the absence of saturation region. TLM structures were also tested to get the contact resistance and sheet resistance.

5.3 Conclusion and future directions

In this section, efforts are made to bring together the results described in the previous section and set the roadmap for future research in this area:

- Interface state density, breakdown voltage of thermal grown silicon dioxide have been evaluated by C-V and I-V measurements;
- Breakdown voltage of PECVD deposited silicon nitride have been evaluated by C-V and I-V measurements;
- Polycrystalline silicon has been obtained through doping and annealing of PECVD grown amorphous silicon; poly-Si was used as the gate of MOSFET in this research;

- Poly-Si gate self-aligned MOSFET has been fabricated and characterized at SFU IMMR fabrication facilities;
- Interface state density of gate oxide was also obtained from calculation by measuring the threshold voltage of MOSFET

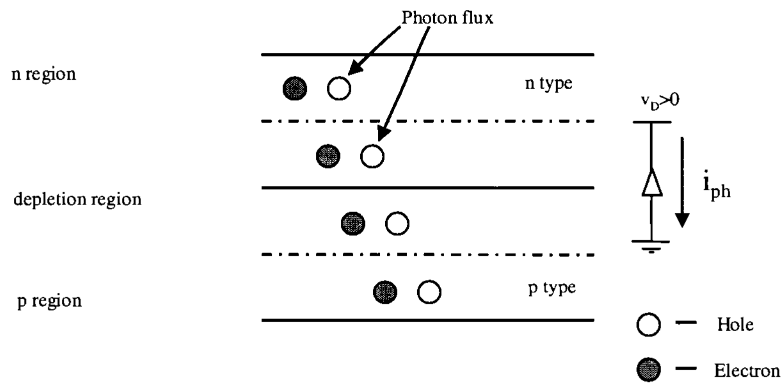
In the future work, attentions should be put on the following aspects:

- Gate oxide: get lower interface state;
- Poly-Si gate: prevent cracking and peeling off during crystallization;
- MOSFET: fabricate MOSFET that is enhancement-mode and can reach saturation;
- APS and PPS array: fabrication and characterize APS and PPS arrays.

APPENDIX 1 APS AND PPS SENSORS

1.1 Parameters determining image sensors

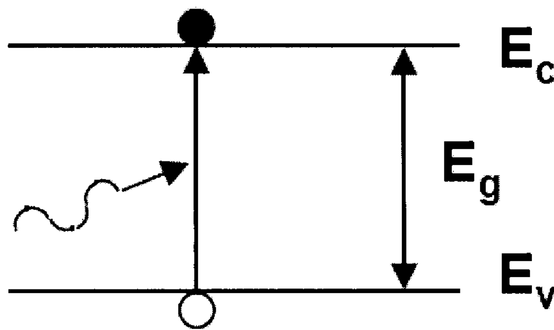
Image sensors form the core of electronic cameras and detectors. The main reason to choose a solid-state camera is to interface it with other machines; in particular, digital analysis, recording or transmission systems. These machines are very limited in the type and speed of operations they can perform. Two primary image sensors dominate the market: CCD (Charge Coupled Device) and CMOS (Complementary MOS) based sensors. An area image sensor array consists of $n \times m$ pixels, ranging from 320×240 to 7000×9000 (very high end astronomy sensor). Photodetector devices serve as the readout of pixel. The photodetector converts the incidental incoming light to photocurrent, which is proportional to the power of radiation. There are several types of photodetectors, the most commonly used is the photodiode: a reverse biased p-n junction, and the photogate: a MOS capacitor [41]. Figure below shows the generation of photocurrent in a reverse biased photodiode. With the development of fabrication techniques, the pixel dimension has reduced from $15 \times 15 \mu m^2$ down to $3 \times 3 \mu m^2$. There are several elements that determine the operation of an optical sensor. We will discuss them in this section.



Generation of photocurrent in photodiode.

Absorption coefficient

As incident light impinges the semiconductor sample, the electrons in the sample will be elevated out of their original sites. If the energy of the photons, $E = hf$, is greater than the bandgap between conduction band E_c and valence band E_v, electrons will be excited to the conduction band, which creates pairs of electron-hole. Figure below is a typical energy diagram for this process.



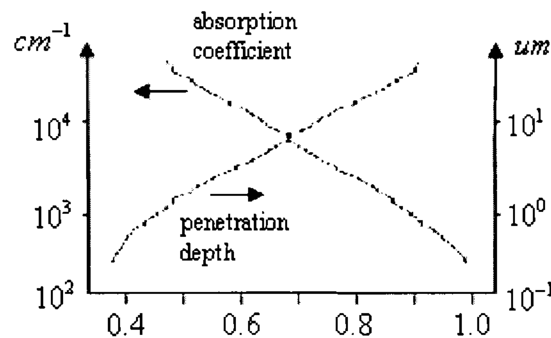
Band diagram of optical absorption

If we consider an incremental slice of material, dx, the change of intensity of light, dI, due to absorption is [42]

$$dI = \alpha \cdot Idx \qquad \text{(Appendix-1)}$$

α is the absorption coefficient, and I is photons/ (cm^2S).

The relations of wavelength versus absorption coefficient and penetration depth are depicted in Figure below. From the curves we can see that α is wavelength dependent.



Relations of absorption coefficient and penetration depth vs. wavelength.

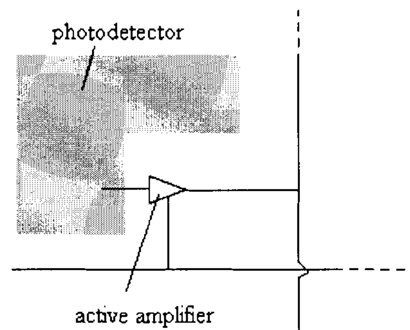
Quantum efficiency

Absorption coefficient describes the percentage of incoming light that can be absorbed by semiconductor. Usually, one photon can generate one electron-hole pair. While, in the case of high energy photons, the energy is enough to generate more than one electron-hole pairs.

The quantum efficiency of the internal photoelectric effect is defined as the number of electron-hole pairs arising from the absorption of one photon [43]. The quantum efficiency number depends on the energy of the photons absorbed. The average number of electron-hole pairs depends on two major elements. One is the primary photon absorption process that generates excited electron and holes. The other is the relaxation process that dissipates the excess energy.

Fill factor

A sensor pixel is composed by photodetector and other necessary circuitry. The percentage of a pixel devoted to collecting light is called the pixel's fill factor, as shown in Figure below, which indicates one pixel of the sensor. A high fill factor is desired in the pixel to pursue high sensitivity. A longer exposure time is needed if the fill factor of pixel is too low. One method to promote the fill factor is to decrease the area of pixel circuitry during layout design.



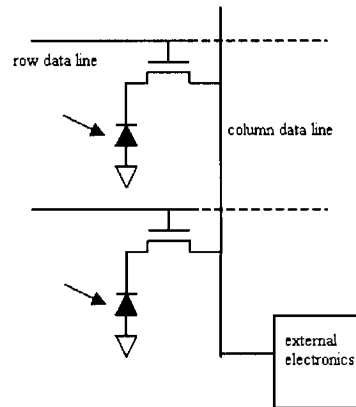
Fill factor refers the percentage of pixel that is sensitive to light.

1.2 APS and PPS

CMOS image sensors can use the advanced standard CMOS technology for fabrication and thus build the fully integrated sensor system on a single chip. This technology requires a lower voltage than CCDs [44], and guarantees superior image quality. CMOS imaging technologies can support two types of photo elements: the photogate and the photodiode. Generally, photodiode sensors are more sensitive, especially to blue light, which can be important in making color cameras. There are two basic types of CMOS sensors – PPS (Passive Pixel Sensor) and APS (Active Pixel Sensor).

Passive Pixel Sensor

A brief illustration of PPS array is shown in Figure below. Each pixel in the PPS consists of a photodetector (e.g. photodiode) and a switch. The switch can be a TFT (Thin Film Transistor) or a MOSFET. In this work, we adopt MOSFET as the switch for the PPS array. In a PPS, the photodetector converts photons to electrical charges. These charges are then transferred by the data line and amplified by a series of charge amplifiers. The amplified signals are then collected and processed by external electronics.



Passive pixel sensor.

There are three modes of operation for the PPS: integration mode, readout mode and reset mode. When the light source reaches the pixel, the photons generate electrical signal charges by introducing the electron-hole pairs. These charges accumulate in the pixel during the integration mode.

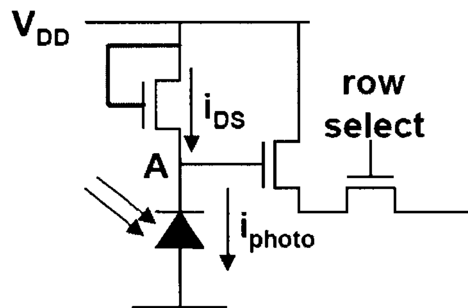
After integration, the charges are transferred to the charge amplifier via column data lines, resulting in the simultaneous occurrence of readout and reset modes. During the charge transfer, the MOSFET switch should be "ON" to let the charges pass through. At the same time, the pixel capacitance is reset to a steady state, value of which is

determined by the positive input of the charge integration [45]. Then there starts another round of integration, readout and reset.

The main disadvantage of this readout technique is the time required to reset the diode fully through the transistor, especially for application in large array. A charge amplifier could be introduced to prevent the potential incomplete reset, which would reduce the dynamic range of the sensor. Noise is another issue that limits the image quality of PPS. While, despite the drawbacks, the fill factor of PPS is maximized because there is only one transistor in pixel.

Active Pixel Sensor

The typical schematic of APS pixel is provided in Figure below. We can see from the figure that the basic form of APS employs the familiar photodiode and a readout circuit of three transistors [42].

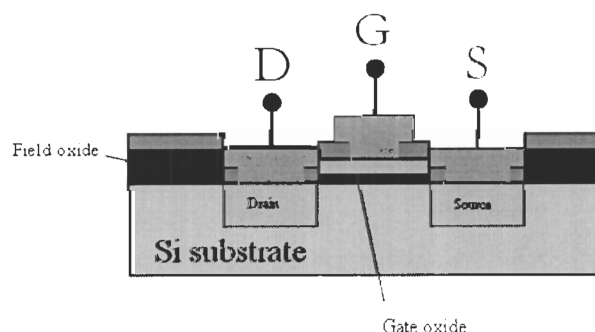


Basic form of APS.

APS can be designed to have high charge to voltage conversion ratios and low read noise, but since high gain requires a small and effective feedback capacitance, it often suffers from large gain fixed pattern noise (FPN). This noise is because of the large relative variation in the size of small feedback capacitors.

APPENDIX 2 MOSFET THEORY

The FET (Field-Effect-Transistor) is a three terminal electronic device in which the current between two terminals, called the "source" and the "drain", is controlled by the potential on a third terminal, called the "gate". The basic structure of MOSFET is shown in Figure below. A conceptually similar structure was first proposed and patented by Lilienfeld and Heil [46] in 1930, but was not successfully demonstrated until 1960. The main technological problem was the control and reduction of the surface states at the interface between the oxide and the semiconductor.



Basic MOSFET structure.

Because it can be scaled down to an extremely small size, thousands of devices can be fabricated in a single integrated circuit. The MOS designation is implicitly used only for the metal-silicon dioxide (SiO_2)-silicon system. The heart of the MOSFET is a MOS capacitor known as a metal-oxide-semiconductor structure.

The MOSFET, in conjunction with other components in circuits, is capable of signal-power gain and voltage gain. Current between the drain and source flows through

a conductive layer under the gate dielectrics, called "inversion layer". The carriers in the inversion layer are of opposite charge to the substrate, which is caused by the gate potential. The gate potential capacitively controls the charge density in the channel, which in turn determines the conductivity between the drain and source [47].

MOS structure capacitor is the key part of a MOSFET. When a proper voltage is applied across the MOS capacitor, the position of the conduction and valence bands relative to the Fermi level at the oxide-semiconductor interface is a function of the MOS capacitor voltage, so that the characteristics of the semiconductor surface can be inverted from p-type to n-type, or vice versa. The operation and characteristics of MOSFET are dependent on this inversion and the creation of an inversion charge density at the semiconductor surface [48].

Based on the inversion layer types, MOSFETs are divided into two major categories: n-channel MOSFET (nMOS), which is fabricated on p-type substrate and electrons are accumulated in the channel; p-channel MOSFET (pMOS), which is fabricated on n-type substrate and holes are accumulated in the channel.

For nMOS, at the very beginning, a positive bias is applied on the gate. The electrons in the substrate will begin to accumulate at the interface of oxide and semiconductor, lead to the generation of a depletion region. Keep increasing the gate bias, more and more electrons will accumulate under the interface. When the gate bias reaches a specific value, called threshold voltage (V_T), the inversion layer will dominate a thin region at the interface in the substrate, the MOSFET enters inversion mode.

When increase the bias applied on gate, V_G, to a specific value, an inversion layer will be created in the interface of oxide and semiconductor. According to V_T, we can

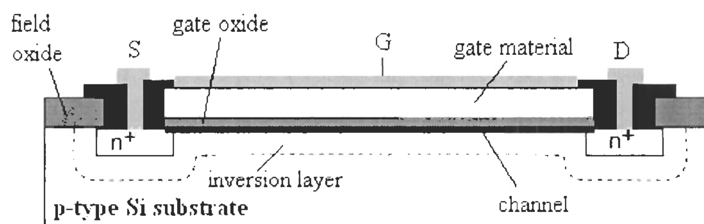
divide the working mode of MOSFET into three regimes: cut-off, linear and saturation regimes. The regimes in nMOS will be discussed in this section.

Cut-off regime

When $V_{GD} < V_T, V_{GS} < V_T$, the inversion layer can not be created, MOSFET is cut-off and there is no electron flow.

Linear regime

When V_G increases till $V_G = V_T$, the thin layer near oxide-semiconductor interface is neutralized by the accumulated electrons. Keep increasing V_G to $V_{GS} > V_T, V_{GD} > V_T$, an inversion layer is created by the accumulated electrons. If a bias, V_{DS}, is applied between drain and source, the electrons in the inversion layer will begin to flow driven by the bias. We call this inversion layer "channel". Figure below shows the MOSFET that works linear regime.



Geometry of MOSFET working in linear regime.

Saturation regime

After the MOSFET reaches linear regime, I_{DS} increases linearly as the V_G increases. While, if we keep increasing the V_D, the voltage between gate and drain, V_{GD}, will decrease, which leads the drain-end of the inversion layer becoming thinner and thinner. Pinch-off will occur when V_D is large enough to make $V_{GD} < V_T$. After pinch-off occurs, the MOSFET will become saturated and I_{DS} will keep constant at value of I_{DSsat}.

Current can only flow in the channel direction, which can be given as

$$J_y = Q_n(y) \cdot v_y(y) \quad \text{(Appendix-2)}$$

Total channel current:

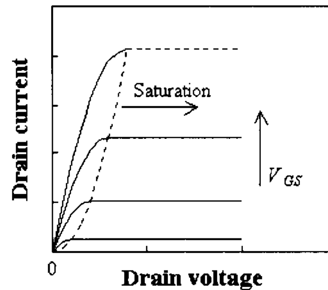
$$I_y = W \cdot Q_n(y) \cdot v_y(y) \quad \text{(Appendix-3)}$$

The relation between I_D-V_{DS} can be deduced as [34]

$$I_D = \frac{\mu_n W C_{ox}}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \quad \text{(Appendix-4)}$$

This equation is valid only if $V_{GS} - V_{DS} \geq V_T$.

From the I_D-V_{DS} equation, the relation of channel current and drain-source voltage can be shown in the Figure below.



ID versus VDS curves for an nMOSFET.

APPENDIX 3 TECHNOLOGY FILE FOR MASK DESIGN

The technology file used in the mask design is listed below.

```
;********************************
; LAYER DEFINITION
;********************************
layerDefinitions(
techPurposes(
;( PurposeName              Purpose#   Abbreviation )
;( -----------              --------   ------------ )
;User-Defined Purposes:
;System-Reserved Purposes:
( warning                 234        wng          )
( label                   237        lbl          )
( error                   239        err          )
( annotate                240        ant          )
( drawing                 252        drw          )
( net                     253        net          )
( cell                    254        cel          )
( all                     255        all          )
) ;techPurposes
techLayers(
;( LayerName                Layer#     Abbreviation )
;( ---------                ------     ------------ )
;User-Defined Layers:
( sub                     1          sub          )
( active                  2          active       )
( mo                        3          mo           )
( sin                     4          sin          )
( al                5          al           )
( background              254        backgro      )
( text                    230        text         )
)  ;techLayers
techLayerPurposePriorities(
;layers are ordered from lowest to highest priority
;( LayerName                Purpose     )
;( ---------                -------     )
( background              drawing     )
( sub                     net         )
( active                  drawing     )
( mo                drawing     )
( sin                     drawing     )
( al                drawing     )
( text                    drawing     )
) ;techLayerPurposePriorities
techDisplays(
;( LayerName    Purpose      Packet          Vis Sel Con2ChgLy DrgEnbl
Valid )
;( ---------    -------      ------          --- --- --------- -------
----- )
```

```
( background   drawing     background      t nil t nil t )
( sub          net         background      t nil t nil nil )
( active       drawing     active          t t t t t )
( mo           drawing     poly1           t t t t t )
( sin          drawing     metal2          t t t t t )
( al           drawing     metal1          t t t t t )
( text         drawing     text            t t t t t )
) ;techDisplays
techLayerProperties(
;( PropName               Layer1 [ Layer2 ]            PropValue )
)
) ;layerDefinitions

;********************************
; PHYSICAL RULES
;********************************
physicalRules(
mfgGridResolution(
    ( 0.01000 )
) ;mfgGridResolution
) ;physicalRules
```

APPENDIX 4 RCA CLEAN

Contaminants present on the surface of silicon wafers at the start of processing, or accumulated during processing, have to be removed at specific processing steps in order to obtain high performance and high reliability semiconductor devices, and to prevent contamination of process equipment, especially the high temperature oxidation, diffusion, and deposition tubes. The RCA clean is the industry standard for removing contaminants from wafers. Werner Kern developed the basic procedure in 1965 while working for RCA (Radio Corporation of America) - hence the name [49]. There are three steps in sequential for RCA cleaning procedure [50]. Table Appendix-1 lists the functions and solutions needed for standard and modified RCA procedure.

Details of RCA cleaning procedure.

	Function	Temperature & Time	Solutions ratio	
			Bared	Oxidized
RCA 1 (organic clean)	remove organic residue and film	10 min @ 80 ± 5°C	$H_2O : H_2O_2 : NH_4OH = 5 : 1 : 1$	$H_2O : H_2O_2 : NH_4OH = 5 : 1 : 1$
HF Dip (Oxide strip)	remove oxide left by RCA1	30 sec @ 20°C	$H_2O : HF = 10 : 1$	$H_2O : HF = 100 : 1$
RCA 2 (Ionic clean)	remove ionic and heavy metal atoms	10 min @ 80 ± 5°C	$H_2O : H_2O_2 : HCl = 6 : 1 : 1$	$H_2O : H_2O_2 : HCl = 6 : 1 : 1$

Before RCA 1, hydrate wafers in DI water before placing in solution. Heat solution near temperature range, add NH_4OH and then H_2O_2. When temperature

stabilizes in the desired range, put wafers in solution and start timer. The RCA 1 will oxidize the silicon wafer and leave a thin layer oxide film which should be removed.

HF dip is used to strip the thin oxide left by RCA 1. There are two options for this step, depends on what surface condition is wanted. Solution with the ratio of H_2O:HF = 10:1 is used when a pure silicon surface is desired; on the other hand, if the wafer under cleaning has been oxidized, this step could be skipped completely or the solution ratio should be adjusted to H_2O:HF = 100:1 in order to avoid etching of the oxide.

During RCA 2, the addition of HCl will raise temperature of the solution significantly. Knowing this property would help to control the temperature in range.

After RCA clean is done, the wafers are ready to go into furnace for field/gate oxide growth. RCA clean will be repeated several times for additional wafer cleaning in the later steps, e.g. before PECVE Si/SiN_x growth, before boron/phosphorous diffusion.

REFERENCE LIST

[1] Robert A. Street, Ed., *Technology and Applications of Amorphous Silicon*. Berlin: Springer series in materials science, Springer-Verlag, 2000.

[2] Y. Yuan, et.al, "Analysis of breast diseases examination with thermal texture mapping, mammography and ultrasound," *26th Annual International Conference of the Engineering in Medicine and Biology Society*, vol. 1, p. 1166 ~ 1169, 2004.

[3] X. Q. Zhou, H. K. Huang, S. L. Lou, "Authenticity and integrity of digital mammography images," *IEEE Transactions on Medical Imaging*, vol. 20, issue 8, p. 784 ~ 791, Aug. 2001.

[4] M. H. Izadi, K. S. Karim, "Pixel architectures for digital X-ray imaging in crystalline silicon technology," *IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, May 2004.

[5] D. K. Schroder, *Semiconductor Material and Device Characterization, second edition*. New York: John Wiley & Sons, Inc., 1998.

[6] Y. Tatewaki, K. Matsuda, K. Tanaka, K. Nishizawa, K. Sakiyama, "An MOS test device with the gate electrode emphasized for dielectric breakdown," *Proc. IEEE 1991 Int. Conference on Microelectroic Test Structures*, vol. 4, No. 1, March 1991.

[7] C. J. Frosch and L. Derick, "Surface Protection and Selective Masking During Diffusion in Silicon," *Proceedings of the Electrochemical Society*, p. 547, 1957.

[8] M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, "Stabilization of Silicon Surfaces by Thermally Grown Oxides," *Bell Syst. Tech. J.*, 38, 749, 1959.

[9] J. R. Ligenza and W. G. Spitzer, "The Mechanisms for Silicon Oxidation in Steam and Oxygen," *J. Phys. Chem. Solids*, 14, 131, 1960.

[10] J. R. Ligenza and W. G. Spitzer, "Effects of Crystal Orientation on Oxidation Rates of Silicon in High Pressure Steam," *J. Phys. Chem.*, 65, 2011, 1961.

[11] D. A. Buchanan, "Scaling the gate dielectric: materials, integration and reliability," *IBM J. RES. DEVELOP.*, vol. 43, No. 3, May 1999.

[12] J Suñé, M Nafría, E Miranda, X Oriols, R Rodríguez and X Aymerich, "Failure physics of ultra-thin SiO_2 gate oxides near their scaling limit," *Semicond. Sci. Technol.*, vol. 15, No 5, pp. 445-454, May 2000.

[13] Y. Nishioka, Y. Ohji, T. P. Ma, "Gate-oxide breakdown accelerated by large drain current in n-channel MOSFET's," *IEEE Electron Device Letters*, vol. 12, issue 3, p. 134 ~ 136, March 1991.

[14] V. Mitra, R. Bouderbala, H. Bentarzi, A. Amrouche, "Charge-extraction technique for studying the surface states in MOS devices," *IEEE Transactions on Electron Devices*, vol 40, issue 5, p. 923 ~ 931, May 1993.

[15] H. H. Pham and A. Natham, "A new numerical method for extraction of overlap capacitance in a-Si TFT's," *IEEE Electron Device Letter*, vol. 29, No. 1, Jan 1999.

[16] E. Avni and J. Shappir, "A model for silicon-oxide breakdown under high field and current stress," *J. Appl. Phys.*, vol. 64, no. 2, p. 743, 1988.

[17] M. A. Lieberman, A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing*, Hoboken, N.J.: Wiley, 2005.

[18] R. L. Kubena, "Si MOSFET fabrication using focused ion beams," *IEEE Transactions on Electron Devices*, vol. 31, issue 9, p. 1186 ~ 1189, Sep 1984.

[19] A. Singh, "Self-aligned molybdenum gate MOSFETs," *Indian Journal of Pure & Applied physics*, vol. 19, pp. 707-710, August 1981.

[20] C. Saint, J. Saint, *IC Mask Design*. New York: McGraw Hill, 2002.

[21] R. C. Jaeger, *Introduction to Microelectronic Fabrication*, Reading, Mass. : Addison-Wesley Pub. Co., 1988.

[22] A. M. Miri, "Development of a novel wet etch fabrication technology for amorphous silicon thin film transistors," PhD dissertation, University of Waterloo, Waterloo, ON, Canada, 1995.

[23] J. Scott and J. Olmstead, "A solid-to-solid diffusion technique," *RCA Review*, vol. 35, pp. 357-368, 1965.

[24] S. M. GadelRab, A. M. Miri, "A comparison of the performance and reliability of wet-etched and dry-etched a-Si:H TFTs," *IEEE Transaction on Electron Devices*, vol. 45, issue 2, p. 560 ~ 563, Feb. 1998.

[25] K. P. Cheung, "Gate-oxide degradation from source/drain (S/D) boron diffusion," *Digest of Technical Papers for 1998 Symposium on VLSI Technology*, p.198 ~ 199, June 9~11, 1998.

[26] D.A. Neaman, *Semiconductor Physics and Devices: Basic Principles, third edition.* New York: McGraw-Hill, 2003.

[27] H. Song and K.R. Farmer, "Measuring interface state distributions in ultra-thin MOS capacitors with direct tunnel current leakage," Proc. MRS Symp. R, *Ultrathin SiO_2 and High-K Materials for ULSI Gate Dielectrics*, San Francisco, CA, Apr. 5-9, 1999.

[28] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, New York: Wiley, 1982.

[29] Y. Nakata, T. Itoga, T. Okamoto, T. Hamada and Y. Ishii, "Low-temperature stacked gate insulator by photo oxidation and PECVD for high-performance TFT LCDs," *Sharp Technical Paper*, No. 3, August 2001.

[30] R. N. Ghosh, P. Tobias, S. G. Ejakov and B. Golding, "Interface states in high temperature SiC gas sensing," *Proceedings of IEEE Sensors*, vol. 2, pp. 1120-1125, 2002.

[31] V. V. Afanas'ev, F. Ciobanu, S. Dimitrijev, G. Pensl and A. Stesmans, "Band alignment and defect states at SiC/oxide interfaces," *J. Phys.: Condens. Matter*, vol.16, pp.1839–1856, 2004.

[32] K. Arai, "Progress in R&D of ultra-low-loss power device technologies in Japan," *FED Journal*, Vol. 11 Supplement, 2000.

[33] Y. S. Lin et al., "Interfacial properties of ZrO_2 on silicon," *J. of App. Phys.*, vol. 93, No. 10, May 15, 2003.

[34] R. A. Governal, A. Bonner, F. Shadman, "Effect of system interactions on the removal of total oxidizable carbon from DI water polishing loops," *IEEE Transactions on Semiconductor Manufacturing*, vol. 5, issue 1, p. 70 ~ 73, Feb. 1992.

[35] T. Kiguchi, N. Wakiya, K. Shinozaki and N. Mizutani, "Improvement of C-V characteristics and control of interlayer growth of rare earth oxide stabilized zirconia epitaxial gate dielectrics," *Key Engineering Materials*, vol. 248, pp. 137-142, 2003.

[36] C. I. Duruöz, R. M. Clarke, C. M. Marcus, and J. S. Harris, Jr., "Conduction threshold, switching, and hysteresis in quantum dot arrays," *Physical Review Letters*, vol. 74, No. 16, April 1995.

[37] C. A. Richter and D. R. Stewart, "Metrology for molecular electronics," *Government Microcircuit Applications & Critical Technology Conference (GOMACTECH)*, April 3, 2003.

[38] B. El-Kareh and R. J. Bombard, *Introduction to VLSI Silicon Devices*, Hingham, Mass.: Kluwer Academic Publishers, 1986.

[39] Y. Okazaki et al., "Sub- 1/4-pm dual-gate CMOS technology using in-situ doped polysilicon for nMOS and PMOS gates," *IEEE Transactions on Electron Devices*, Vol. 42, NO. 9, pp. 1583-1590, September 1995.

[40] K. S. Karim, P. Servati, A. Nathan, "High voltage amorphous silicon TFT for use in large area applications," *Microelectronics Journal*, vol. 35, pp. 311-315, 2004.

[41] X.Q. Liu, "CMOS image sensors dynamic range and SNR enhancement via statistical signal processing," PhD dissertation, Stanford University, Stanford, CA, USA, 2002.

[42] M. A. Parker, *Physics of Optoelectronics*, Boca Raton, FL: Taylor & Francis Books Ltd/CRC, 2005.

[43] E. Antončik, and N. K. S. Gaur, "Theory of the quantum efficiency in silicon and germanium," *J. Phys. C: Solid State Phys.*, vol. 11, pp. 735-744, 1978.

[44] B. J. Hosticka, "CMOS sensor systems," *1997 International Conference on Solid State Sensors and Actuators*, vol. 2, p.991 - 994, June 16~19, 1997.

[45] K.S. Karim, "Pixel architectures for digital imaging using amorphous silicon technology," PhD dissertation, University of Waterloo, Waterloo, ON, Canada, 2002.

[46] J.E. Lilienfeld, U.S. Patent 1,745,175 (1930) and O. Heil, British Patent 439,457 (1935)

[47] N. S. J. McLaughlin, "InGaP/InGaAs heterostructure field effect transistor," M. A. Sc. Thesis, Simon Fraser University, Burnaby, BC, Canada, 1999.

[48] K. F. Brennan, A. S. Brown, *The Modern Electronic Semiconductor Devices*. New York: Wiley-Interscience Publication 2002.

[49] W. Kern and J. Vossen, Eds., *Thin Film Processes*. New York: Academic Press, 1978.

[50] W. Kern, Ed., *Handbook of Semiconductor Cleaning Technology*. Park Ridge, NJ: Noyes Publishing, 1993.